LAB MANUAL

ON

ELECTRONIC DEVICES

EC-304

EXPERIMENT NO. 1

AIM:-

To observe and draw the Forward and Reverse bias V-I Characteristics of a P-N Junction diode.

APPARATUS:-

P-N Diode IN4007.
Regulated Power supply (0-30v)
Resistor 1K_
Ammeters (0-200 mA, 0-500mA)
Voltmeter (0-20 V)
Bread board
Connecting wires

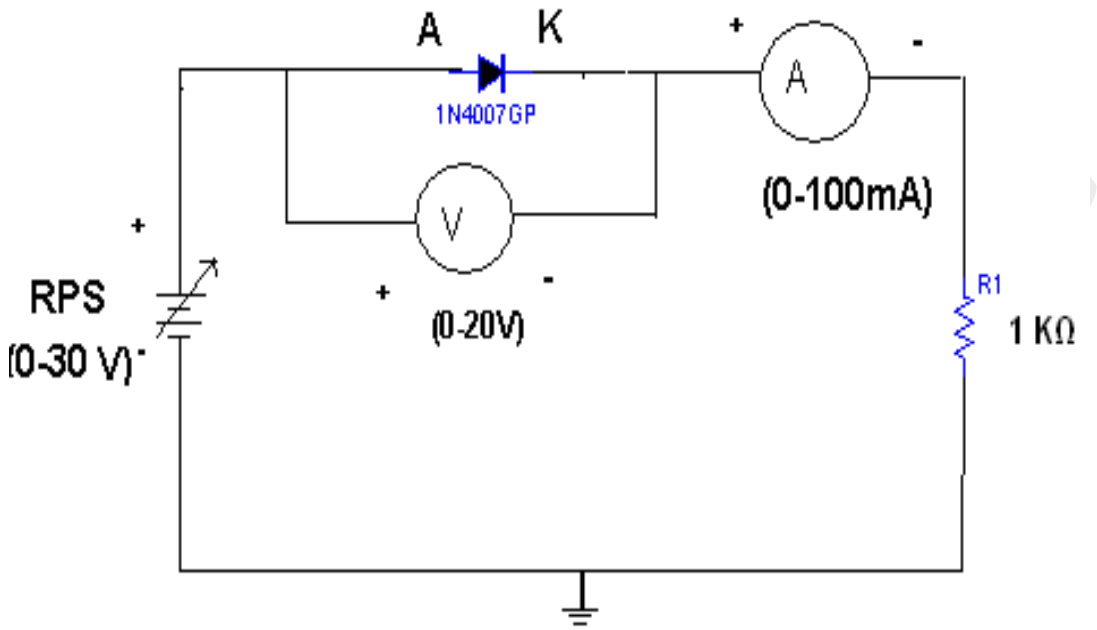
THEORY:-

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

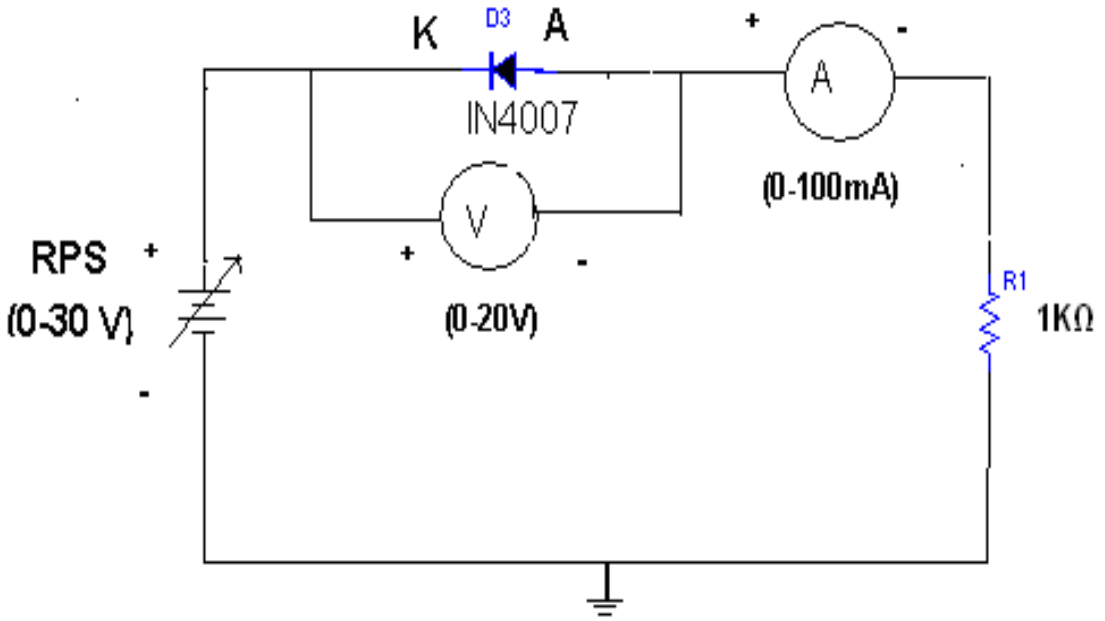
When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carrier.

CIRCUIT DIAGRAMs:-

FORWARD BIAS:-

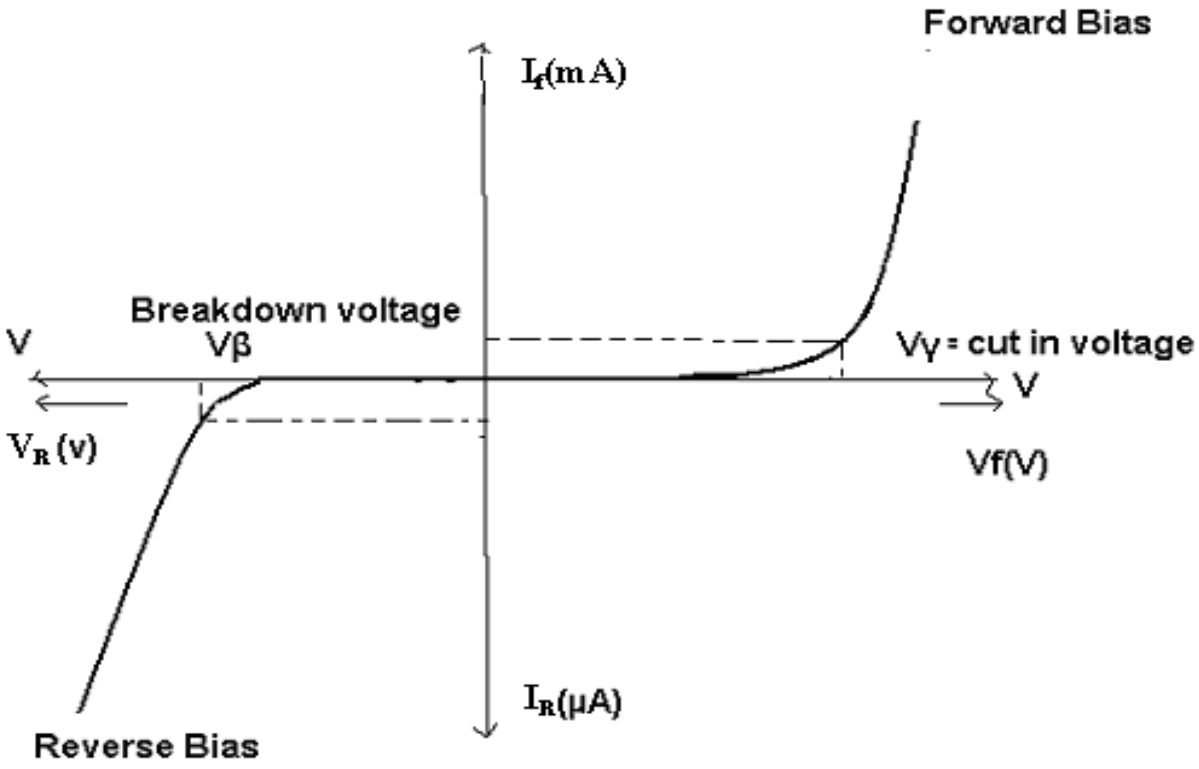


REVERSE BIAS:-



MODEL WAVEFORM:-

PROCEDURE:-



PROCEDURE:-

FORWARD BIAS:-

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode.
3. Switch on the power supply and increases the input voltage (supply voltage) inSteps.
4. Note down the corresponding current flowing through the diode and voltageacross the diode for each and every step of the input voltage.
5. The reading of voltage and current are tabulated.
6. Graph is plotted between voltage and current.

OBSERVATION:-

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE(V)	CURRENT THROUGH DIODE(mA)

PROCEDURE:-

REVERSE BIAS:-

1. Connections are made as per the circuit diagram
2. For reverse bias, the RPS +veis connected to the cathode of the diode andRPS –ve is connected to the anode of the diode.
3. Switch on the power supply and increase the input voltage (supply voltage) inSteps.
4. Note down the corresponding current flowing through the diode voltageacross the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated
6. Graph is plotted between voltage and current.

OBSEVATION:-

S.NO	APPLIED VOLTAGE (V)	VOLTAGE ACROSS DIODE(V)	CURRENT THROUGH DIODE(mA)

PRECAUTIONS:-

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

RESULT: -

Forward and Reverse Bias characteristics for a p-n diode are observed.

EXPERIMENT NO. 2

AIM: -

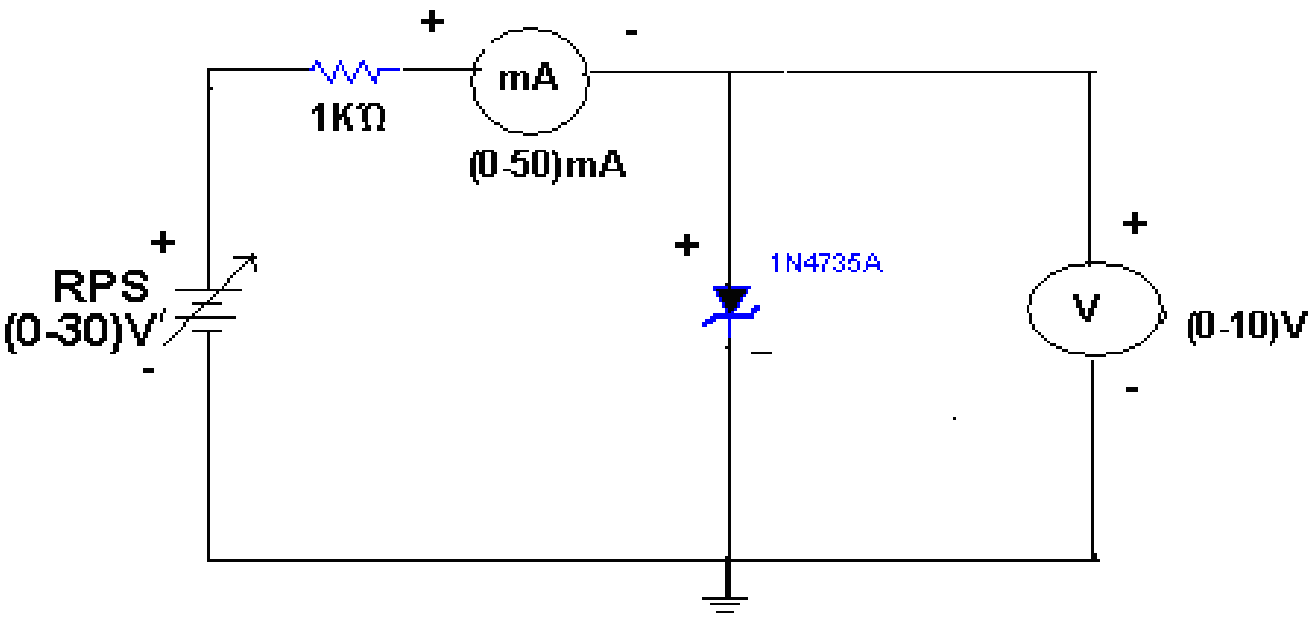
a) To observe and draw the static characteristics of a zener diode.
b) To find the voltage regulation of a given zener diode.

APPARATUS*:* -

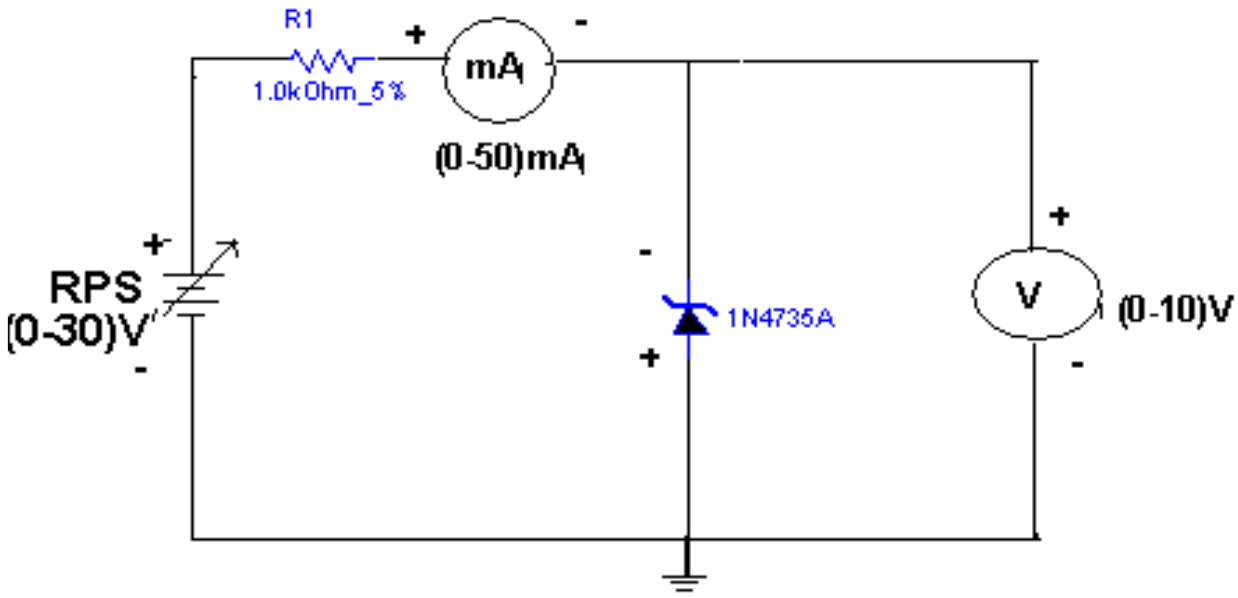
Zener diode
Regulated Power Supply (0-30V)
Voltmeter (0-20V)
Ammeter (0-100mA)
Resistor (1KΩ)
Bread Board
Connecting wires

CIRCUIT DIAGRAM:-

STATIC CHARACTERISTICS:-



REGULATION CHARACTERISTICS:-



Theory:-

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device To avoid high current, we connect a resistor in series with zener diode.

Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

PROCEDURE:-

Static characteristics:-

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.

3. The zener current (lz), and the zener voltage (Vz.) are observed and thennoted in the tabular form.
4. A graph is plotted between zener current (Iz) and zener voltage (Vz).

Regulation characteristics:-

1. The voltage regulation of any device is usually expressed as percentage regulation
2. The percentage regulation is given by the formula

$$((V_{NL}-V_{FL})/V_{FL})X100$$

V_{NL}=Voltage across the diode, when no load is connected.
V_{FL}=Voltage across the diode, when load is connected.

3. Connection are made as per the circuit diagram
4. The load is placed in full load condition and the zener voltage (V_Z), Zener current (l_Z), load current (I_L) are measured.
5. The above step is repeated by decreasing the value of the load in steps.
6. All the readings are tabulated.
7. The percentage regulation is calculated using the above formula

OBSERVATIONS:-

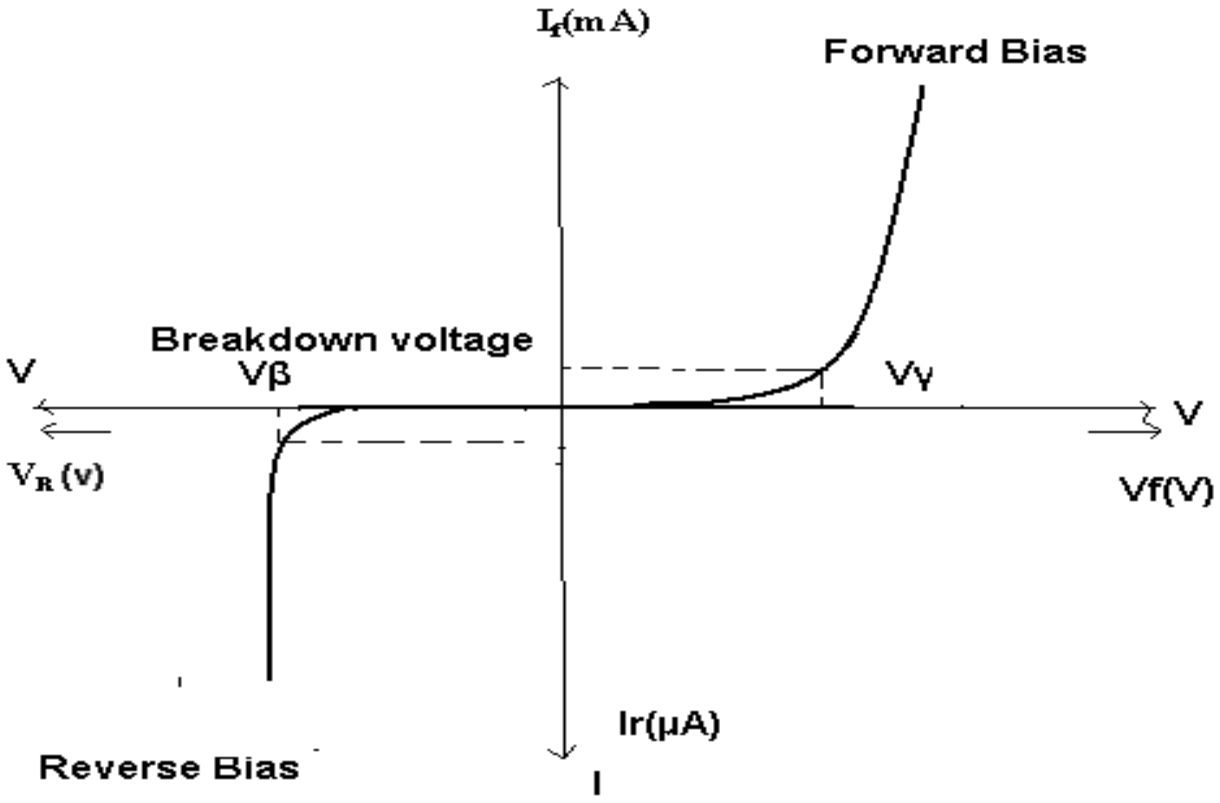
Static characteristics:-

S.NO	ZENER VOLTAGE(V_Z)	ZENER CURRENT(I_Z)

Regulation characteristics:-

S.No.	V_{NL}(VOLTS)	V_{FL} (VOLTS)	R_L(KΩ)	% REGULATION

MODEL WAVEFORMS:-



PRECAUTIONS:-

1. The terminals of the zener diode should be properly identified
2. While determined the load regulation, load should not be immediately shorted.
3. Should be ensured that the applied voltages & currents do not exceed the ratings ofthe diode.

RESULT:-

a) Static characteristics of zener diode are obtained and drawn.
b) Percentage regulation of zener diode is calculated.

EXPERIMENT NO. 3

AIM: -

To examine the input and output waveforms of half wave Rectifier and alsocalculate its load regulation and ripple factor.

1. with Filter
2. without Filter

APPARATUS:-

Bread Board
Multimeters–2No's.
Transformer (6-0-6).
Diode, 1N 4007
Capacitor 100µf.
Resistor 1K.
Connecting wires

THEORY: -

During positive half-cycle of the input voltage, the diode D_1 is in forward bias and conducts through the load resistor R_1. Hence the current produces an output voltage across the load resistor R_1, which has the same shape as the +ve half cycle of the input voltage.

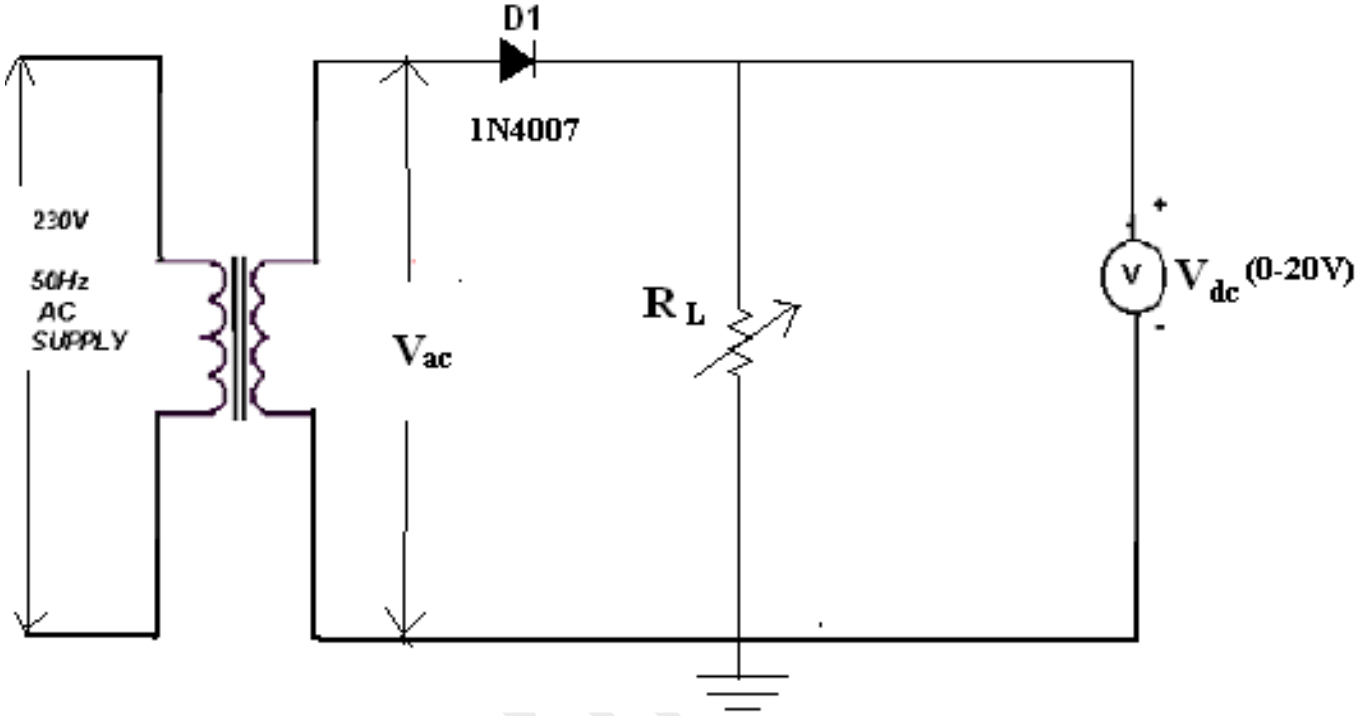
During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

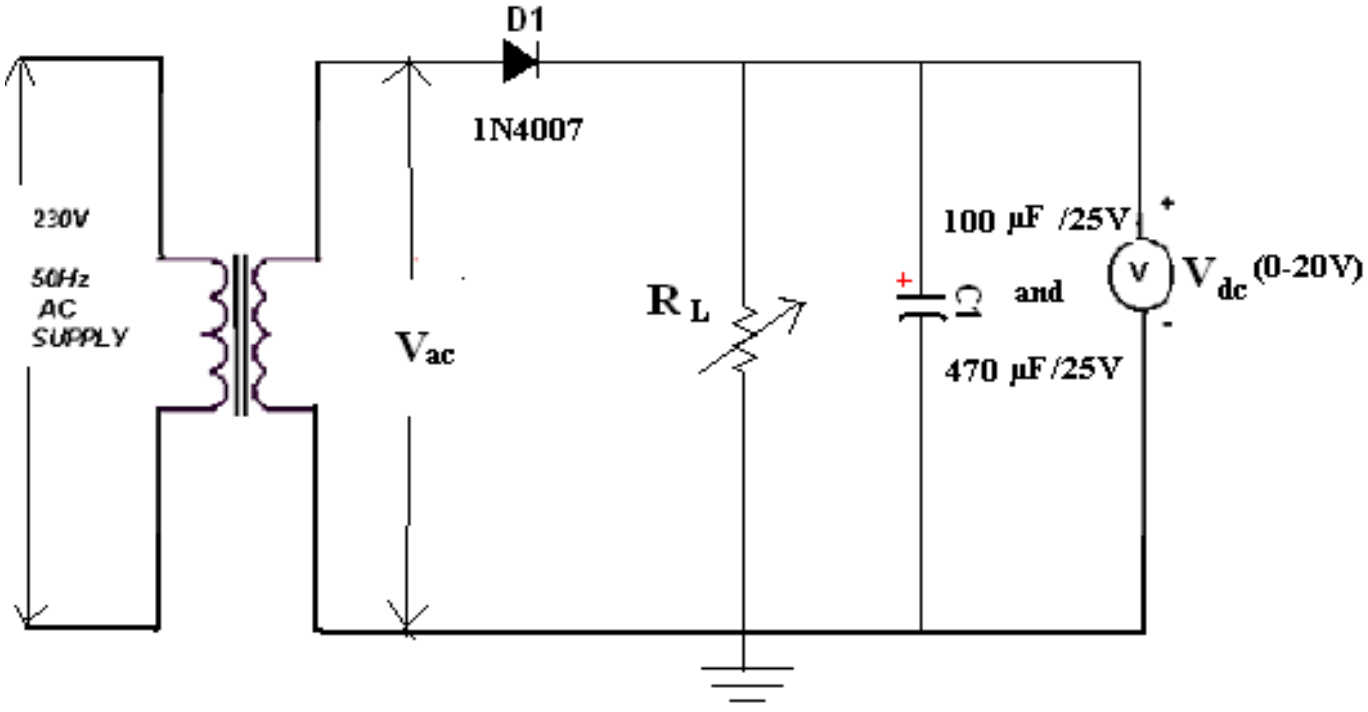
1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazards in the secondary circuit.

CIRCUIT DIAGRAM:-

A) Half wave Rectifier without filter:

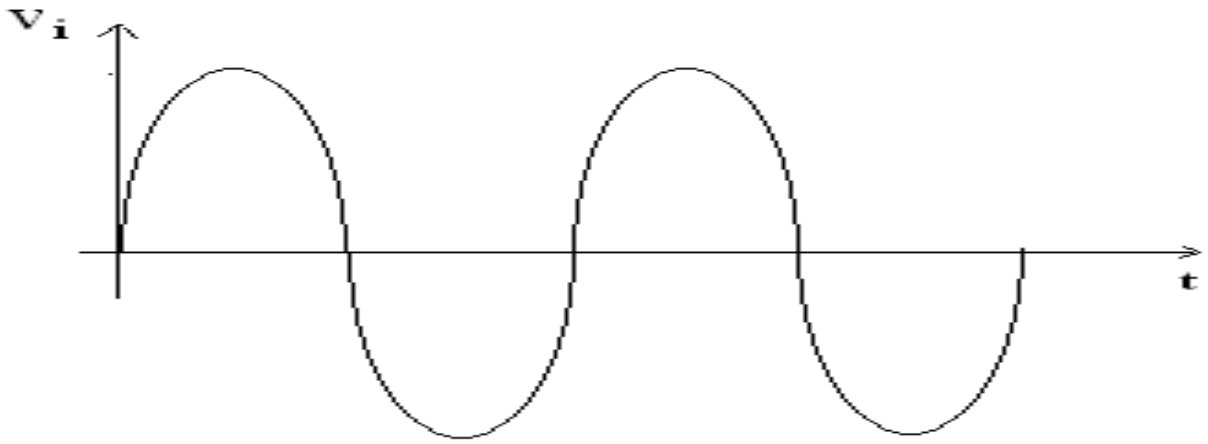


B) Half wave Rectifier with filter

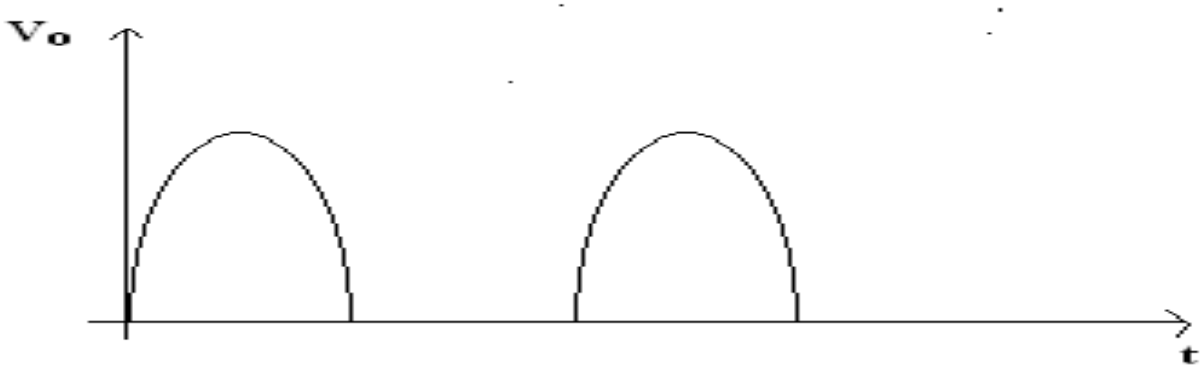


WAVEFORMS:

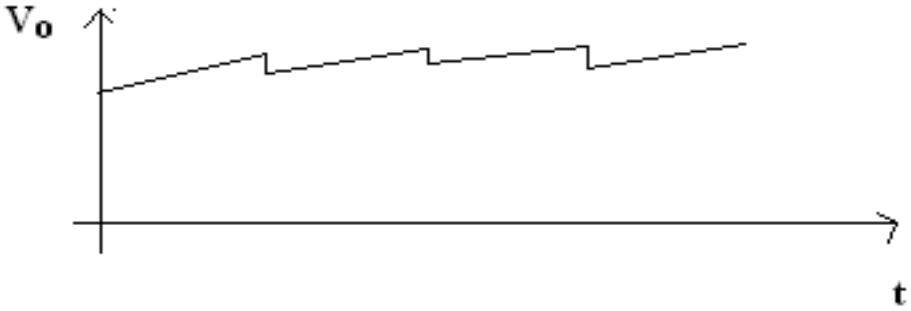
A) INPUT WAVEFORM



B) OUTPUT WAVFORM WITHOUT FILTER



C) OUTPUT WAVEFORM WITH FILTER:



PROCEDURE:-

1. Connections are made as per the circuit diagram.
2. Connect the primary side of the transformer to ac mains and the secondary side to therectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltageat the output of the rectifier.
4. Find the theoretical of dc voltage by using the formula,

$$V_{dc} = \frac{V_m}{\pi}$$

Where,

$$V_m = V_{rms}$$

The Ripple factor is calculated by using the formula

$$r = \frac{ac\ output\ voltage}{dc\ output\ voltage}$$

REGULATION CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. By increasing the value of the rheostat, the voltage across the load and currentflowing through the load are measured.
3. The reading is tabulated.
4. From the value of no-load voltages, the %regulation is calculated using theformula,

$$\%\ Regulation = ((V_{NL} - V_{FL})/V_{FL}) * 100$$

CALCULATIONS:

Theoretical calculations for ripple factor:-

Without Filter:-

$$V_{rms} = \frac{V_m}{2}$$

$$V_{dc} = \frac{V_m}{\pi}$$

$$V_m = V_{rms}$$

$$\textbf{Ripple factor } r = \sqrt{((V_{rms}/V_{dc})^2 - 1)} = 1.21$$

With Filter:-

$$\textbf{Ripple factor } r = \frac{1}{2\sqrt{3fCR}}$$

Where f=50Hz
C =470 μF
R=1K

Practical calculations:-

V_{ac}=
V_{dc}=
Ripple factor without Filter=
Ripple factor with Filter =

OBSERVATION:

	V_m (V)	V_{ac} (V)	V_{dc} (V)	$r = V_{ac}/V_{dc}$
WITHOUT FILTER				
WITH FILTER				

PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified.
2. The polarities of all the diodes should be carefully identified.
3. While determining the % regulation, first Full load should be applied and then itshould be decremented in steps.

RESULT:

The ripple factors for half wave Rectifier with and without load and the loadregulation has been calculated**.**

EXPERIMENT NO. 4

AIM:

To examine the input and output waveforms of Full Wave Rectifier and also calculate its load regulation and ripple factor.

1. with Filter
2. without Filter

APPARATUS:

Bread Board
Multimeters–2No's.
Transformer (6-0-6).
Diode, 1N 4007
Capacitor 100μf.
Resistor 1K.
Connecting wires

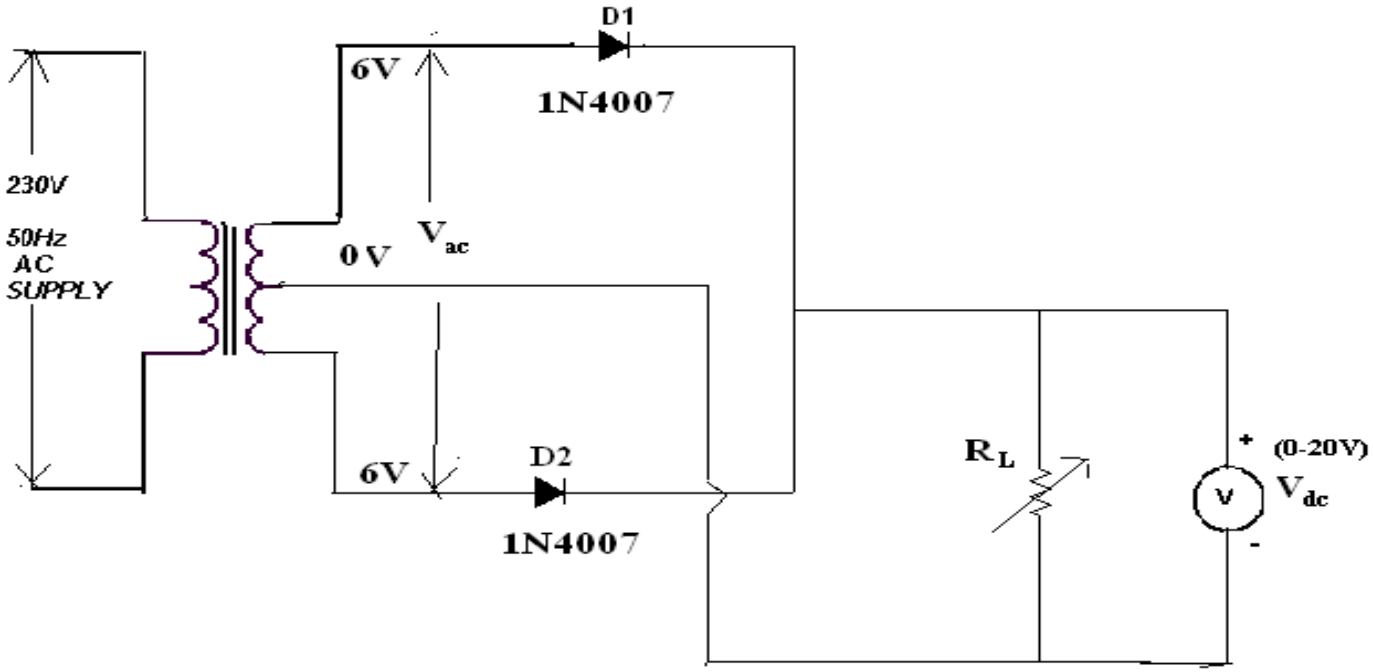
THEORY:

The circuit of a center-tapped full wave rectifier uses two diodes D_1& D_2. During positive half cycle of secondary voltage (input voltage), the diode D_1 is forward biased and $D_2$is reverse biased. So the diode D_1 conducts and current flows through load resistor R_L. During negative half cycle, diode D_2 becomes forward biased and D_1 reverse biased. Now, D_2 conducts and current flows through the load resistor $R_L$in the same direction.

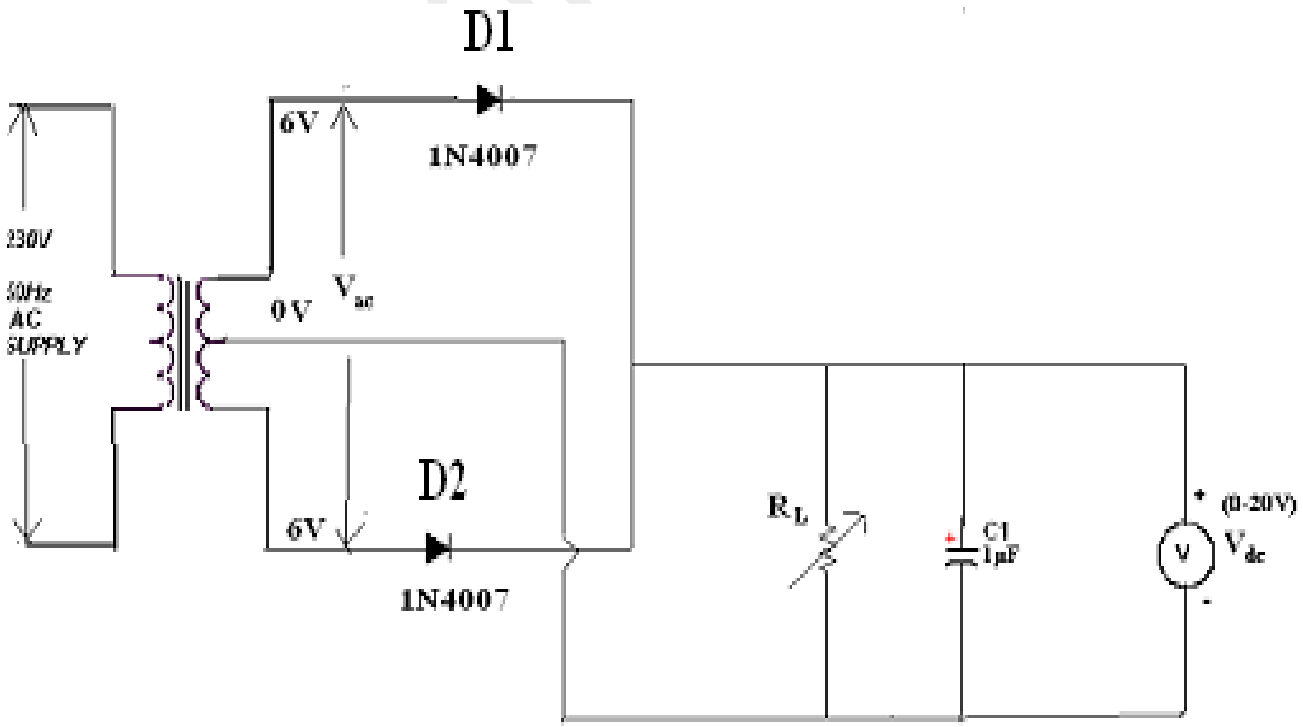
There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a full wave rectifier allows unidirectional (one way) current to the load during the entire 360 degrees of the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

CIRCUIT DIAGRAM:

A) FULL WAVE RECTIFIER WITHOUT FILTER:

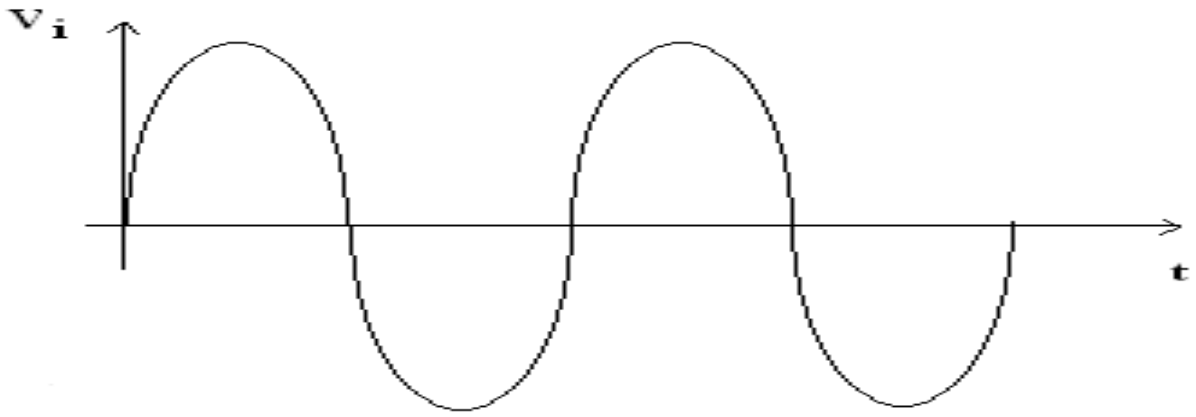


B) FULL WAVE RECTIFIER WITH FILTER:

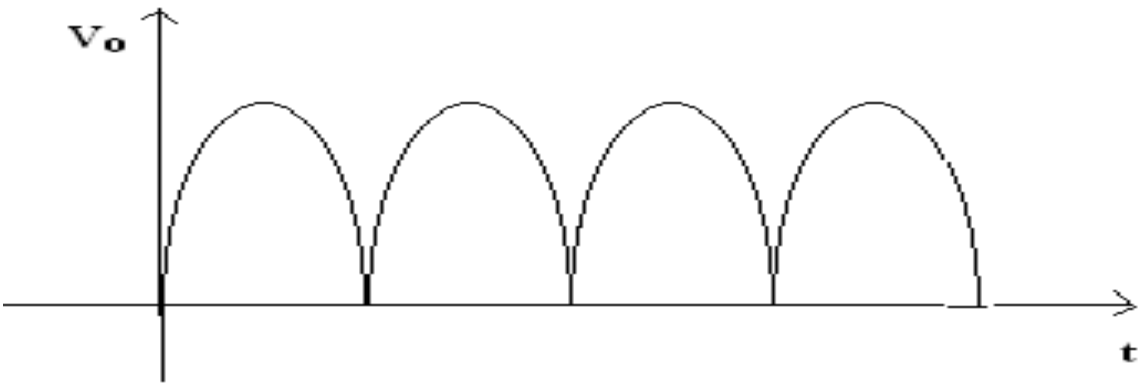


WAVEFORMS:

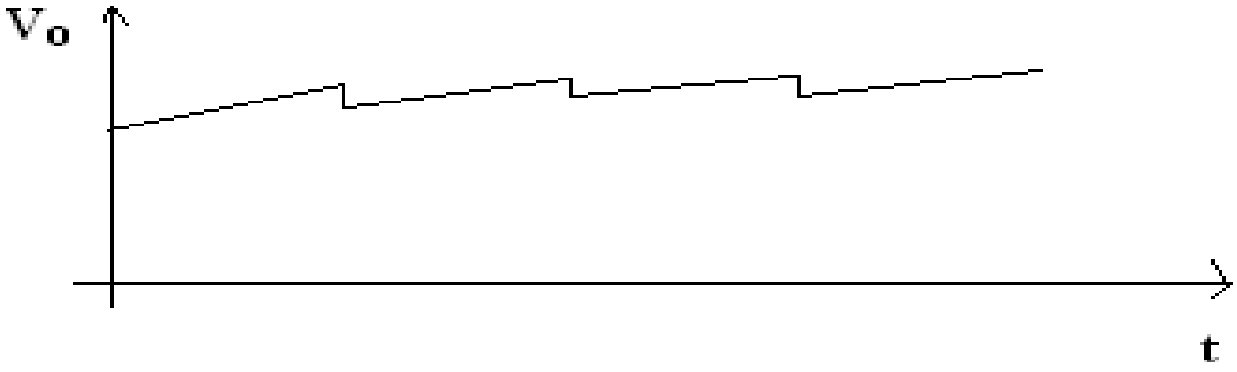
A) INPUT WAVEFORM



B) OUTPUT WAVEFORM WITHOUT FILTER:



C) OUTPUT WAVEFORM WITHOUT FILTER:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Connect the ac mains to the primary side of the transformer and the secondaryside to the rectifier.
3. Measure the ac voltage at the input side of the rectifier.
4. Measure both ac and dc voltages at the output side the rectifier.
5. Find the theoretical value of the dc voltage by using the formula

$$\boldsymbol{V_{dc} = \frac{2V_m}{\pi}}$$

6. Connect the filter capacitor across the load resistor and measure the values of$\boldsymbol{V_{ac}}$ and $\boldsymbol{V_{dc}}$at the output.
7. The theoretical values of Ripple factors with and without capacitor arecalculated.
8. From the values of $\boldsymbol{V_{ac}}$ and $\boldsymbol{V_{dc}}$ practical values of Ripple factors arecalculated. The practical values are compared with theoretical values.

CALCULATIONS:
Theoretical calculations:

$$\boldsymbol{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

$$\boldsymbol{V_{dc} = \frac{2V_m}{\pi}}$$

$$\boldsymbol{V_m = V_{rms}\sqrt{2}}$$

1. **Without filter**:

$$\boldsymbol{Ripple\ factor\ r\ = \sqrt{((V_{rms}/V_{dc})^2 - 1)} = 0.812}$$

2. **With filter**:

$$\boldsymbol{Ripple\ factor\ r = \frac{1}{4\sqrt{3fCR}}}$$

Practical calculations:-

$\boldsymbol{V_{ac}}$ =
$\boldsymbol{V_{dc}}$ =
Ripple factor without Filter =
Ripple factor with Filter =

OBSERVATION:

	V_m (V)	V_{ac} (V)	V_{dc} (V)	$r = V_{ac}/V_{dc}$
WITHOUT FILTER				
WITH FILTER				

PRECAUTIONS:

1. The primary and secondary side of the transformer should be carefully identified.
2. The polarities of all the diodes should be carefully identified.

RESULT:

The ripple factors for Full wave Rectifier with and without load and the loadregulation has been calculated**.**

EXPERIMENT NO. 7

AIM:

1. To observe and draw the input and output characteristics of a transistor connected in common base configuration.
2. To find α of the given transistor and also its input and output Resistances.

APPARATUS REQUIRED:

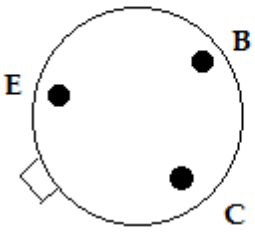
Bipolar Junction Transistor
Resistor 1 kΩ,
Voltmeter (0 – 20V)
Ammeter (0 – 10mA)
2 Regulated Power Supplies (0 – 30V)
Bread Board
Connecting wires required

FORMULA USED:

- Input Impedance = $\Delta V_{EB} / \Delta I_E$ Ω
- Output Admittance = $\Delta I_C / \Delta V_{CB}$ mho
- Current Gain = $\Delta I_C / \Delta I_E$
- Voltage Gain = $\Delta V_{CB} / \Delta V_{EB}$

BJT PIN DIAGRAM

SL100 or BC107



E-Emitter
B-Base
C-Collector

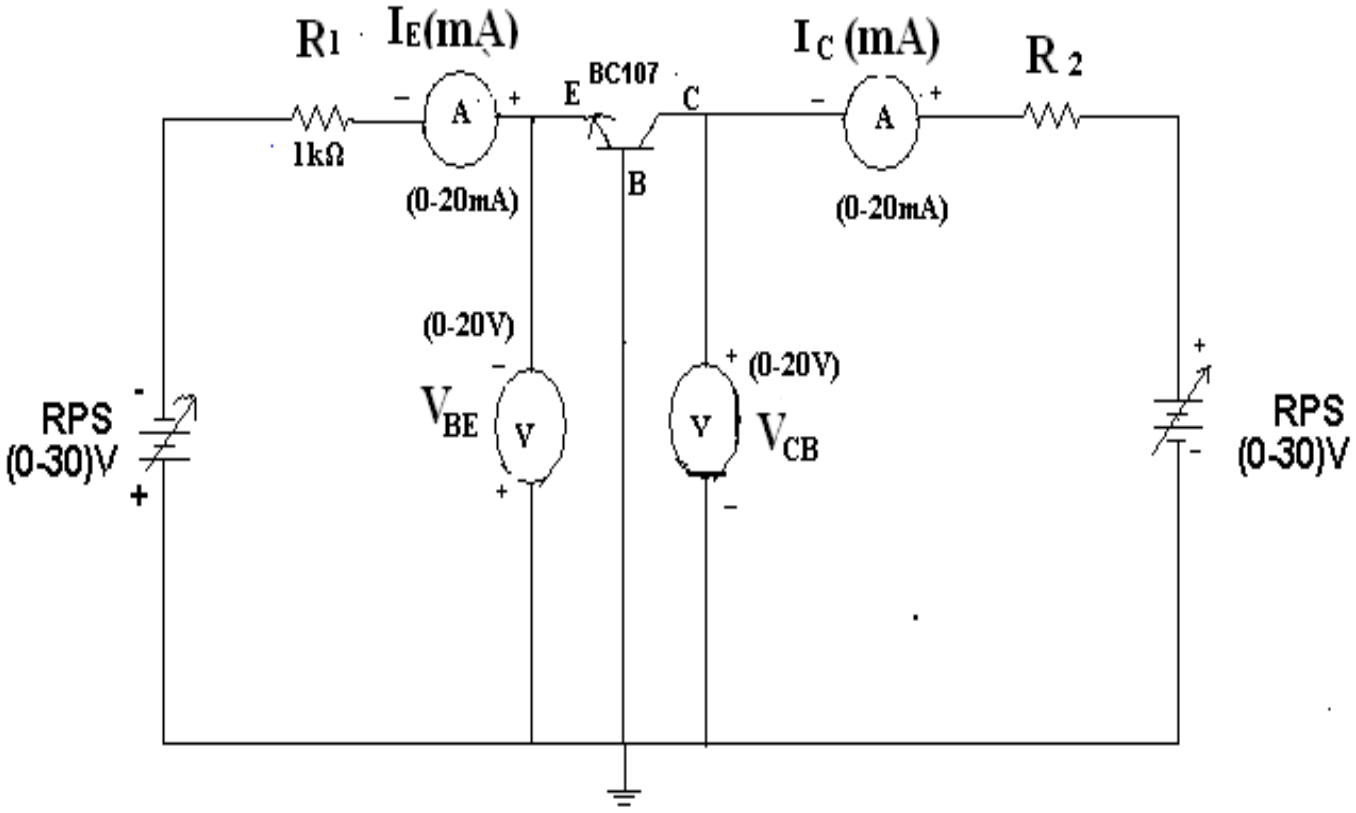
THEORY:

Bipolar Junction Transistor (BJT) is a three-terminal semiconductor device capable of amplifying an ac signal. The three terminals are called the emitter, the base, and the collector. The device is made up three "layers" of p-type and n-type semiconductor material. BJTs consist of a thin base layer (either P- or N-type) sandwiched between two layers of the opposite type material. Thus, BJTs are either NPN or PNP. They are somewhat like two interconnected, back to back diodes, with two diode junctions.

In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased. The input characteristics are plots of I_E versus V_{BE} at constant values of V_{CB}. These characteristics will look like diode characteristics, particularly if the collector is shorted to the emitter and the emitter-base junction is forward biased.

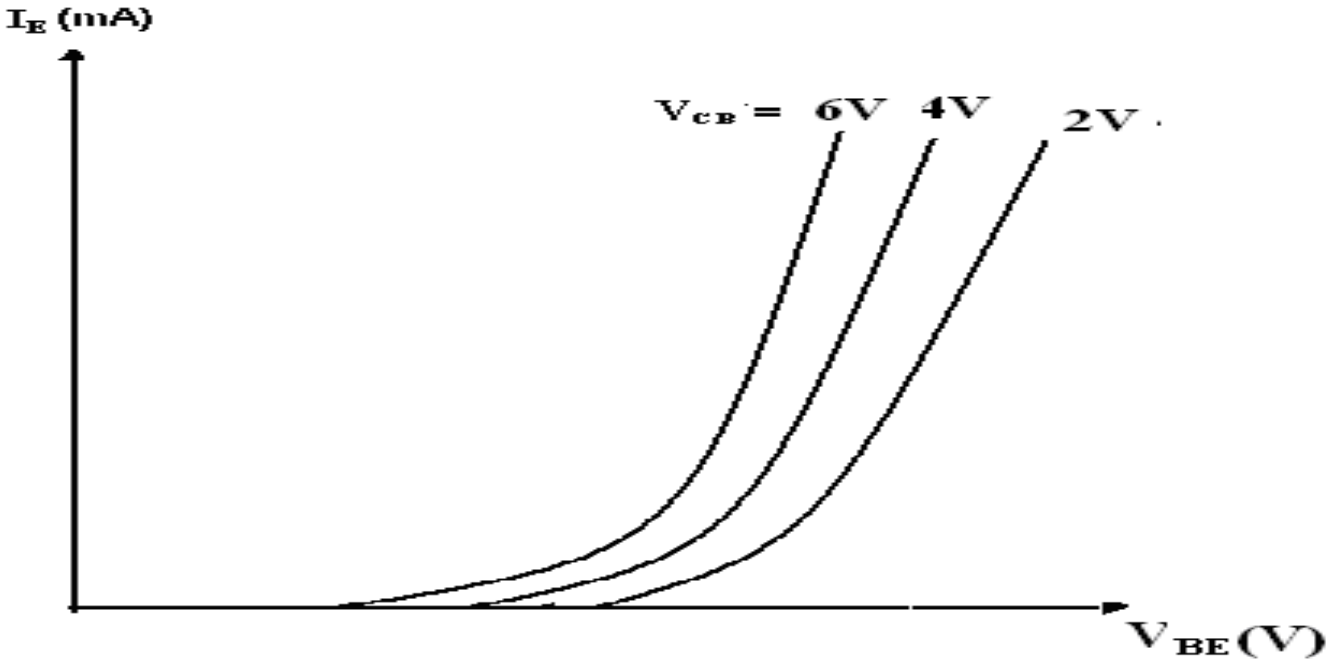
The output characteristics, often called the collector characteristics, are plots of I_C versus V_{CB} at constant values of I_E.

CIRCUIT DIAGRAM:

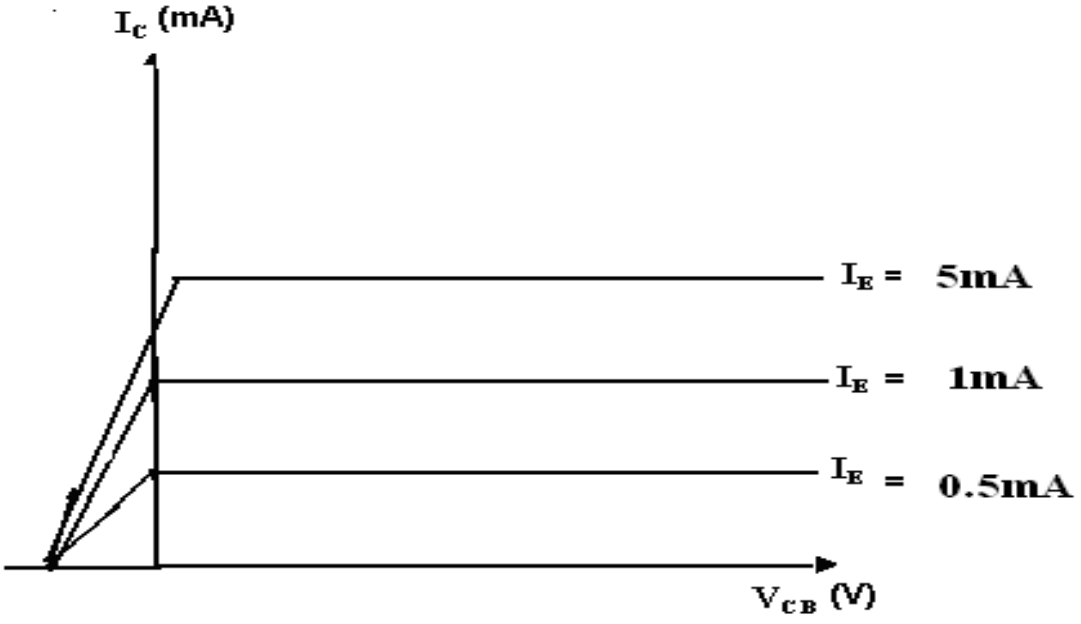


CHARACTERISTICS CURVE:

A) INPUT CHARACTERISTICS



B) OUTPUTCHARACTERISTICS



PROCEDURE:

A) INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics, the output voltage V_{CE} is kept constant at 0V and for different values of V_{EE} ,note down the values of IE and VBE
3. Repeat the above step keeping V_{CB} at __V, __V, and __V and all the readings are tabulated.
4. A graph is drawn between V_{EB} and I_E for constant V_{CB}.

B) OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E is kept constant at __mA and for different values of V_{CC}, note down the values of I_C and V_{CB}.
3. Repeat the above step for the values of I_E at __mA, __mA and all the readings are tabulated.
4. A graph is drawn between V_{CB} and $I_c$for constant I_E

OBSERVATIONS:

(A)INPUT CHARACTERISTICS:

S. No.	VEE (V)	VCB= V		VCB= V		VCB= V	
		VEB (V)	IE (mA)	VEB (V)	IE (mA)	VEB (V)	IE (mA)

(B)OUTPUT CHARACTERISTICS:

S. No.	VCC (V)	IE = mA		IE = mA		IE = mA	
		VCB (V)	IC (mA)	VCB (V)	IC (mA)	VCB (V)	IC (mA)

PRECAUTIONS:

1. The supply voltages should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

RESULT:

The Current gain of the Transistor in CB is _____ , the input Resistance is _____ and the output Resistance is _____.

EXPERIMENT NO. 8

AIM:

1. To draw the input and output characteristics of transistor connected in CE configuration
2. To find β of the given transistor and also its input and output Resistances

APPARATUS:

Transistor, BC107	-	1No.
Regulated power supply (0-30V)	-	1No.
Voltmeter (0-20V)	-	2No.
Ammeter (0-20mA)	-	1No.
Ammeter (0-200μA)	-	1No.
Resistor, 100Ω	-	1No
Resistor, 1KΩ	-	1No.
Bread board		
Connecting wires		

FORMULA USED:

- Input Impedance = $\Delta V_{EB} / \Delta I_B$ Ω
- Output Admittance = $\Delta I_C / \Delta V_{CE}$ mho
- Current Gain = $\Delta I_C / \Delta I_B$
- Voltage Gain = $\Delta V_{CE} / \Delta V_{EB}$

THEORY:

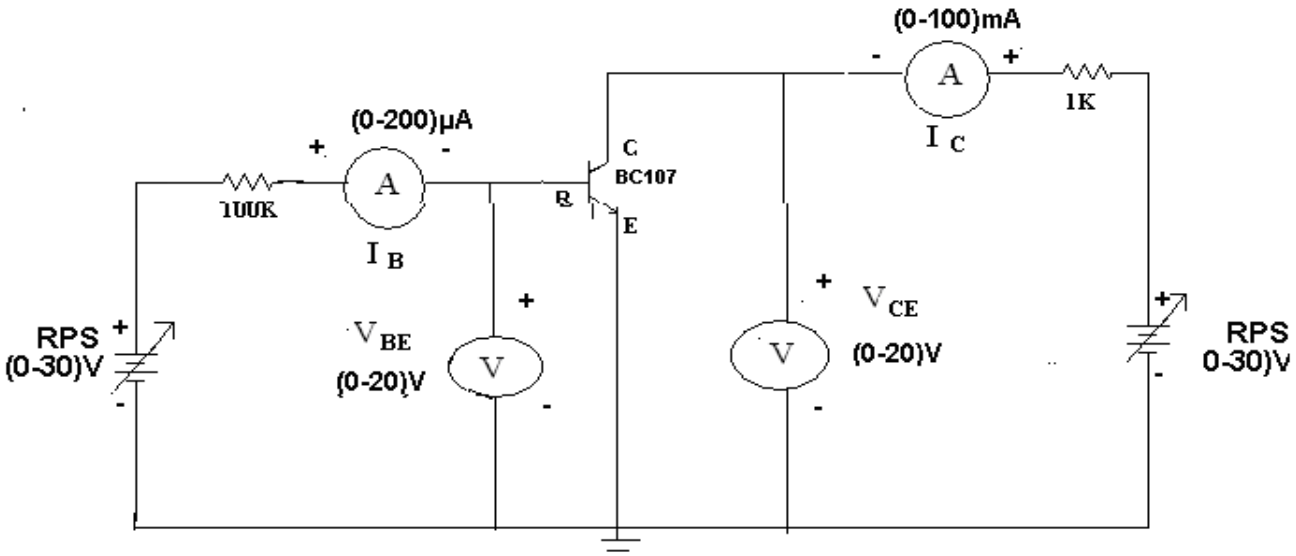
In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE}at constant I_B. the collector current varies with V_{CE}up to few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE}up to

whichthe collector current changes with V CE is known as Knee voltage. The transistor always operated in the region above Knee voltage, IC is always constant and is approximately equal to IB.The current amplification factor of CE configuration is given by

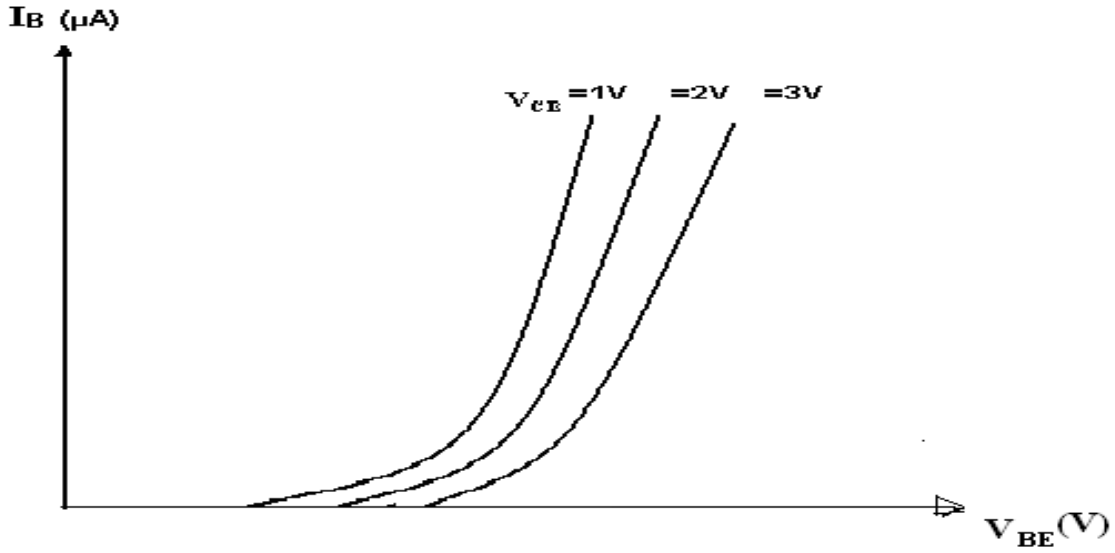
$$\beta = \Delta I_C / \Delta I_B$$

CIRCUIT DIAGRAM:

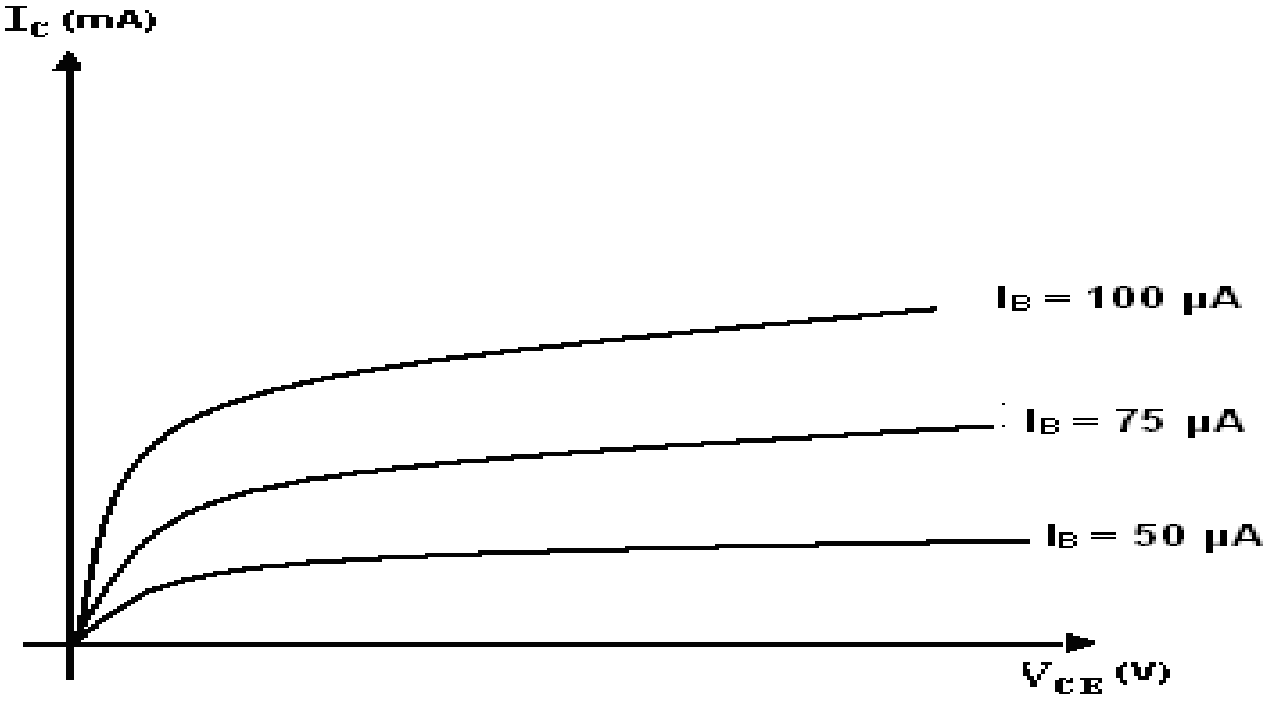


CHARACTERISTICS CURVE:

A) INPUT CHARACTERISTICS:



B) OUTPUT CHARACTERSITICS:



PROCEDURE:

A) INPUT CHARACTERISTICS

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage VCE is kept constant at 1Vand for different values of VBB , note down the values of IB and VBE
3. Repeat the above step by keeping VCE at 2V and 4V and tabulate all the readings.
4. plot the graph between VBE and IB for constant VCE

B) OUTPUT CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram
2. for plotting the output characteristics the input current IB is kept constant at50µA and for different values of VCC note down the values of IC and VCE
3. Repeat the above step by keeping IB at 75 µA and 100 µA and tabulate the all thereadings
4. plot the graph between VCE and IC for constant IB

OBSERVATIONS:

A) INPUT CHARACTERISTICS:

S. No.	VBB (V)	VCE = V		VCE = V		VCE = V	
		VBE (V)	IB (μA)	VBE (V)	IB (μA)	VBE (V)	IB (μA)

A) OUTPUT CHARACTERISTICS:

S. No.	VCC (V)	IB = μA		IB = μA		IB = μA	
		VCE (V)	IC(mA)	VCE (V)	IC(mA)	VCE (V)	IC(mA)

PRECAUTIONS:

1. The supply voltage should not exceed the rating of the transistor.
2. Meters should be connected properly according to their polarities.

RESULT:

The input and output characteristics of transistor connected in CE configuration have been observed and the β of the transistor is calculated as ____ and its input and output Resistances are _____ and _____.

EXPERIMENT NO. 9

AIM:

To draw the V-I Characteristics of SCR

APPARATUS:

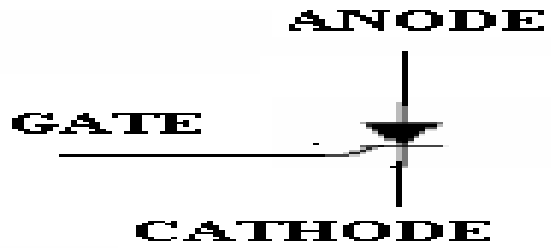
SCR (TYN616)	-1No.
Regulated Power Supply (0-30V)	-2No.
Resistors 10kΩ, 1kΩ	-1No.Each one
Ammeter (0-50) μA	-1No.
Voltmeter (0-10V)	-1No.
Breadboard	-1No .
Connecting Wires.	

THEORY:

It is a four layer semiconductor device being alternate of P-type and N-type silicon. Itconsists of 3 junctions J1, J2, J3 the J1 and J3 operate in forward direction and J2 operates in reverse direction and three terminals called anode A, cathode K, and a gate G. The operation of SCR can be studied when the gate is open and when the gate is positive with respect to cathode.

When gate is open, no voltage is applied at the gate due to reverse bias of the junction J2 no current flows through R2 and hence SCR is at cut off.

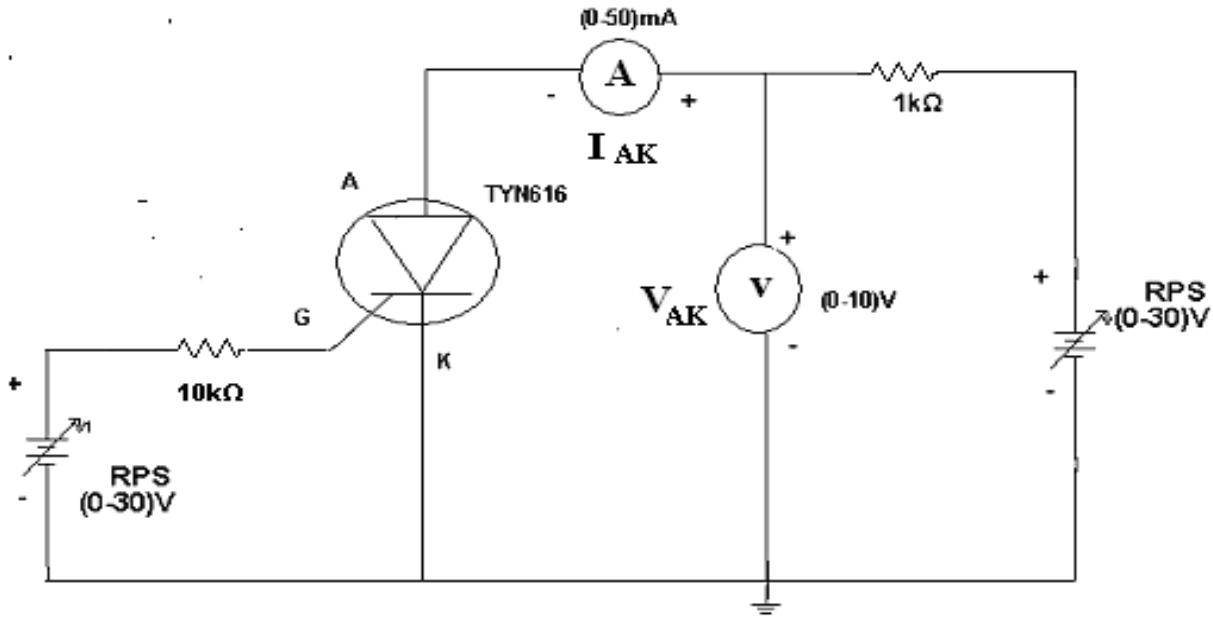
When anode voltage is increased J2 tends to breakdown. When the gate positive, with respect to cathode J3 junction is forward biased and J2 is reverse biased .Electrons from N-type material move across junction J3 towards gate while holes from P-type material moves across junction J3 towards cathode. So gate current starts flowing, anode current increase is in extremely small current junction J2 break down and SCR conducts heavily.



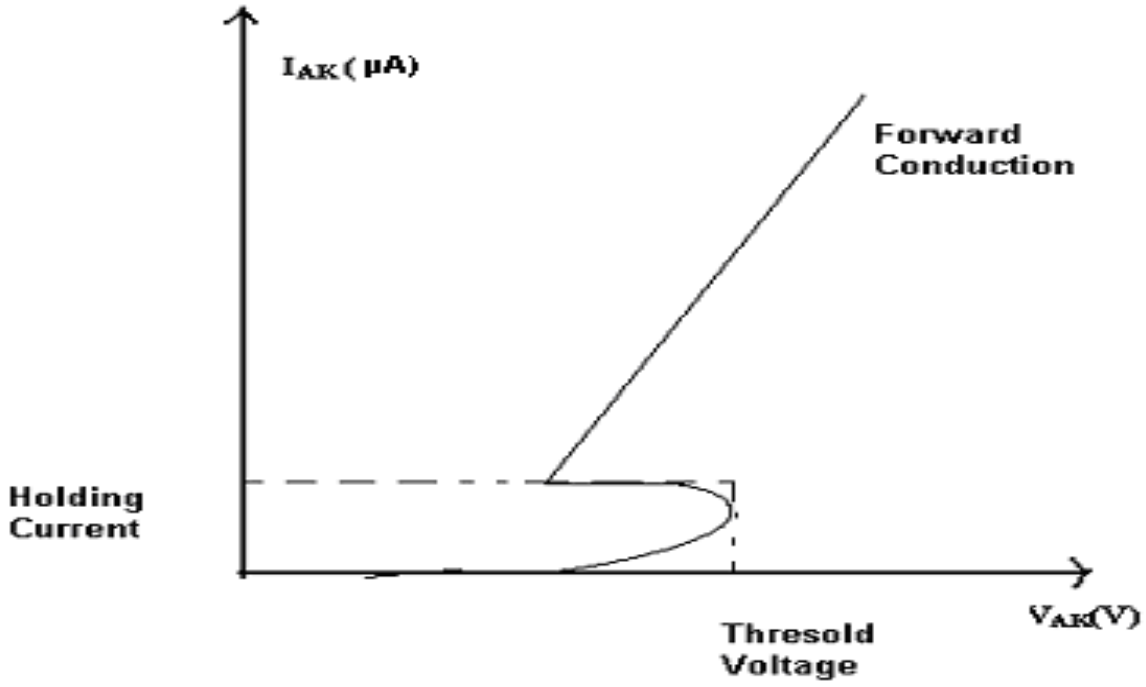
SCR SYMBOL

When gate is open thee break over voltage is determined on the minimumforward voltage at which SCR conducts heavily. Now most of the supply voltage appears across the load resistance. The holding current is the maximum anode current gate being open, when break over occurs.

CIRCUIT DIAGRAM:



V-I CHARACTERISTICS:



OBSERVATION:

V_{AK}(V)	I_{AK}(μA)

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Keep the gate supply voltage at some constant value.
3. Vary the anode to cathode supply voltage and note down the readings of voltmeter and ammeter. Keep the gate voltage at standard value.
4. A graph is drawn between VAK and IAK.
5. From the graph note down the threshold voltage and Holding current values.

CALCULATIONS:

Threshold Voltage =
Holding Current =

RESULT:

The V-I Characteristics of the SCR have been plotted.

EXPERIMENT NO. 10

AIM:

To observe the characteristics of UJT and to calculate the Intrinsic Stand-Off Ratio (η).

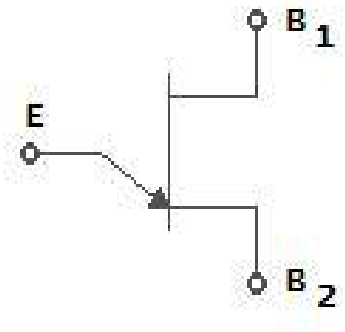
APPARATUS:

Regulated power supply (0-30V)	-2Nos
0-20V (DMM)	-2Nos
0-20mA (DMM)	-1No.
Resistors 1Kohm	-2Nos
Resistor 470 ohm	-1No.
Breadboard	
Connecting wires	

THEORY:

A Unijunction Transistor (UJT) is an electronic semiconductor device that has only one junction. The UJT Unijunction Transistor (UJT) has three terminals anemitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of ptype and it is heavily doped.

The resistance between B1 and B2, when the emitter is open-circuit is called interbase resistance. The original Unijunction transistor, or UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length. The 2N2646 is the most commonly used version of the UJT.

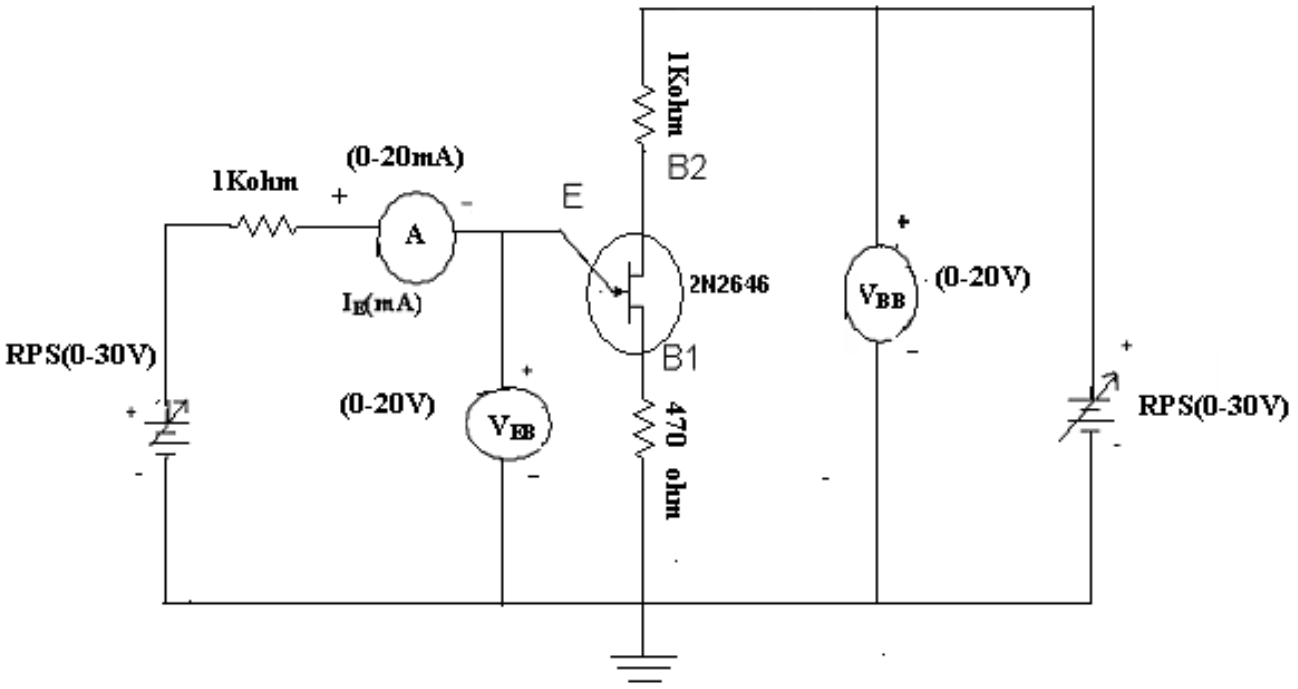


Circuit symbol

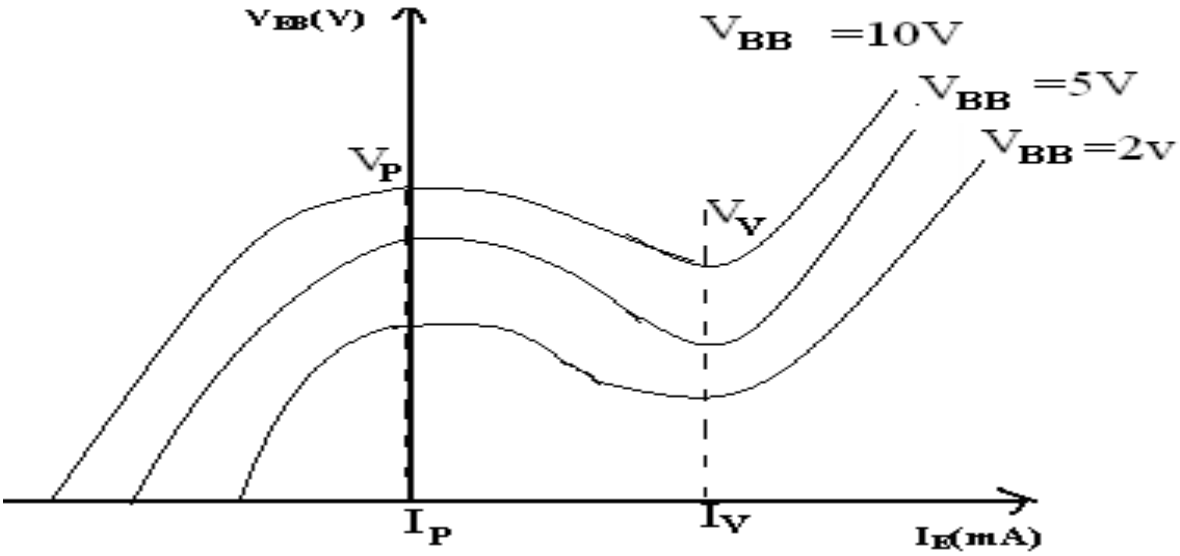
The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current (actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected.

Overall, the effect is a negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. Hence the emitter voltage reaches V_P, the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point; R_{B1} reaches minimum value and this region,V_{EB} proportional to I_E.

CIRCUIT DIAGRAM:



V-I CHARACTERISTICS:



PROCEDURE:

1. Connection is made as per circuit diagram.
2. Output voltage is fixed at a constant level and by varying input voltagecorresponding emitter current values are noted down.
3. This procedure is repeated for different values of output voltages.
4. All the readings are tabulated and Intrinsic Stand-Off ratio is calculated using

$$\eta = \frac{(V_P - V_D)}{V_{BB}}$$

5. A graph is plotted between V_{EE} and I_E for different values of V_{BE}.

CALCULATIONS:

$$V_P = \eta V_{BB} + V_D$$

$$\eta = \frac{(V_P - V_D)}{V_{BB}}$$

$$\eta = \frac{\eta_1 + \eta_2 + \eta_3}{3}$$

OBSEVATIONS:

V_{BB}(v)		V_{BB}(v)		V_{BB}(v)	
V_{BE}(v)	I_E(mA)	V_{BE}(v)	I_E(mA)	V_{BE}(v)	I_E(mA)

RESULT:

The Intrinsic Stand-Off Ratio (η) of the UJT is _____.

EXPERIMENT NO. 6

AIM:

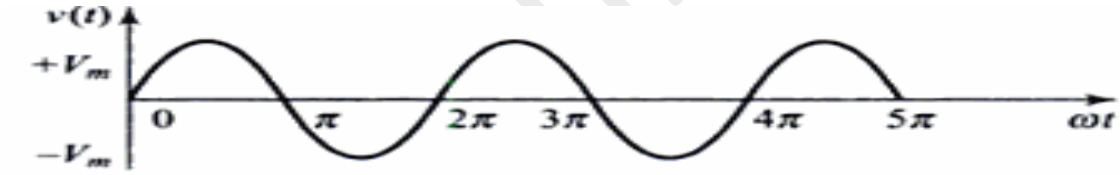
To observe waveforms at the output of clamper circuits

APPARATUS:

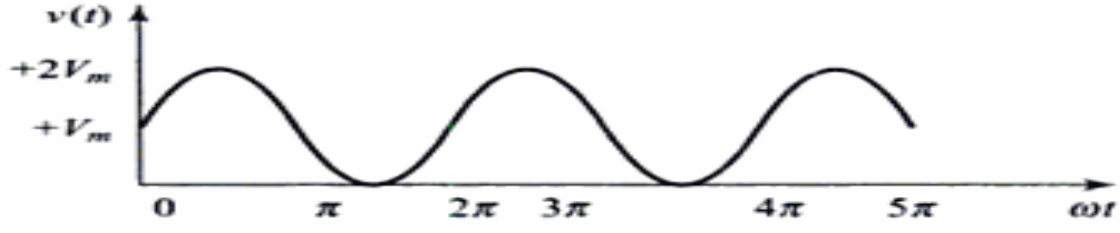
Diode
Capacitor 470 μF
CRO
CRO PROBES
Resistor 1 kΩ
Breadboard
Connecting wires

THEORY:

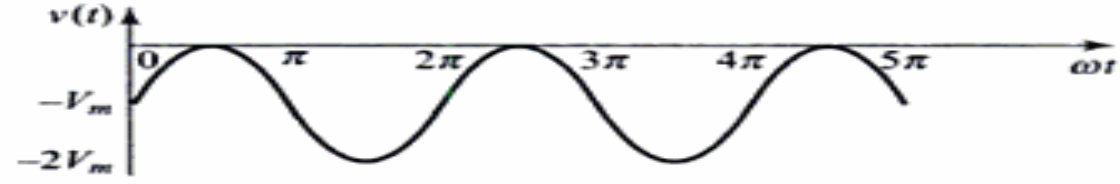
Diodes are widely used in clipping and clamping circuits. Clamping circuits are used to change DC level (average level) of the signal which adds or subtracts DC value with the signal. In clamping, shape of waveform remains same only offset value (DC level) will change. Positive clamping adds positive DC level in the signal while negative clamping adds negative DC level in the signal. Capacitor is widely used in the clamping circuit. Typical clamping waveforms for the sinusoidal signal are shown below for positive clamping and negative clamping.



Sinewave with average value 0



Sine wave clamped to postive level Vm



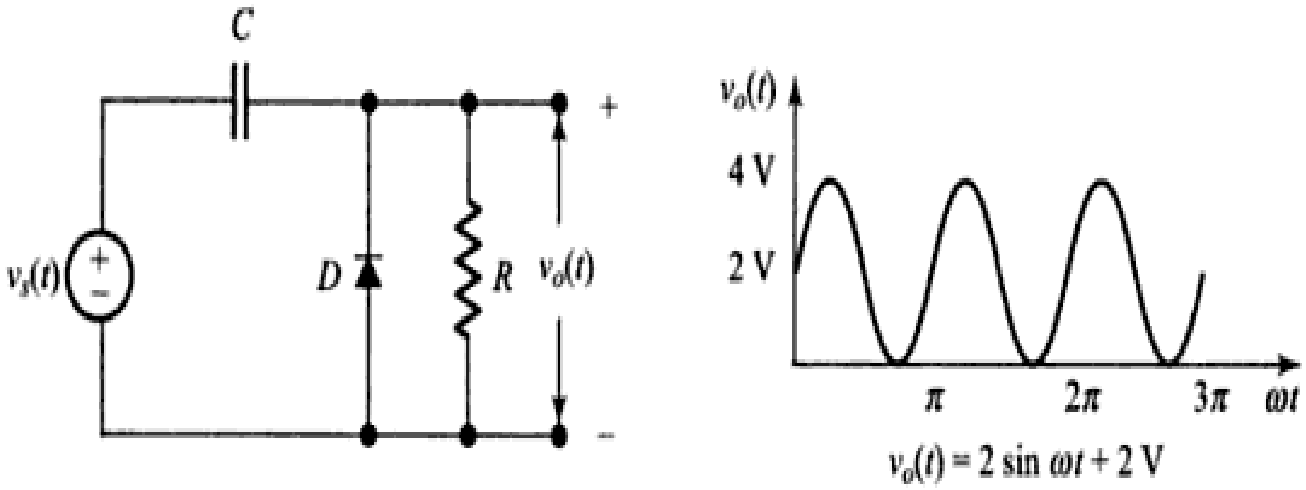
Sine wave clamped to negative level -Vm

Clamping circuit is used in video amplifier of television receiver to restore DC level of video signal to preserve overall brightness of the scene. Clamping circuit is also used in offset control of function generator. Zero offset means no DC value is added in the AC signal.

Circuit Operation:

Typical circuit operation of the positive clamping and negative clamping is given below.

Positive clamping:

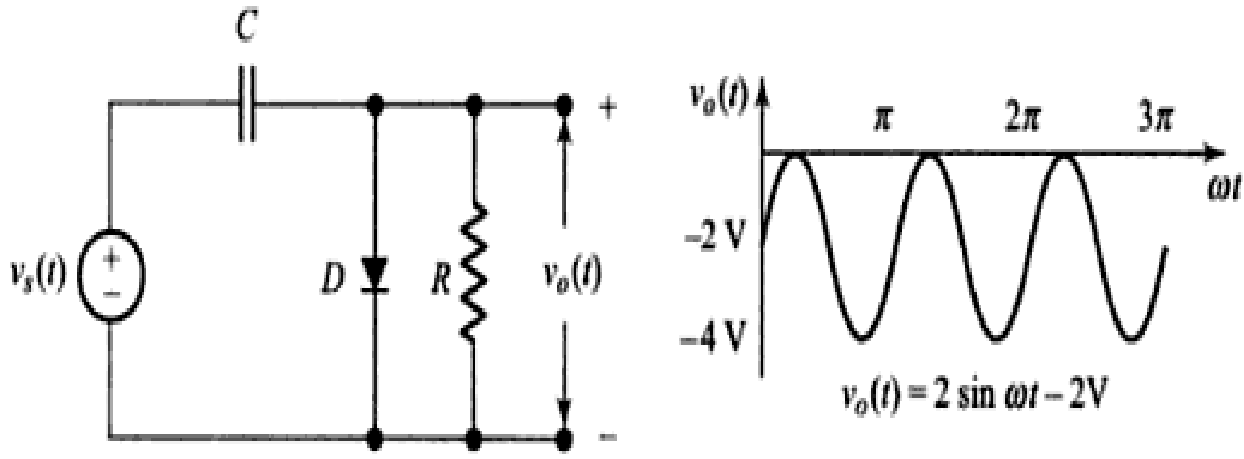


Consider that 4V peak to peak signal with zero offset is applied at the input of the clamping circuit. On the first negative half cycle of the input signal, diode D turns ON because anode voltage is greater than cathode voltage. Capacitor charges to the negative peak voltage let us say -2V in our example. The value of R should be high so that it will not discharge the capacitance.

After completion of negative cycle, positive cycle starts and diode turns OFF. Capacitance voltage is in series with the input voltage. As per the Kirchoff's law output voltage will be addition of input voltage and capacitance voltage. Input signal is positive swing of +2V and capacitor voltage is +2V. Thus during the positive peak of the input voltage total output voltage will be +4V. We can consider that during the positive cycle capacitor acts like a battery and adds +2V in the input.

Waveforms are drawn here considering ideal diode, no leakage in the capacitance under ideal situations which will be different in practical situations.

Negative clamping:



In a negative clamping circuit polarity of diode is reverse than in positive clamping. In our signal input swings from -2V to +2V (peak to peak 4V). Diode turns ON during the positive cycle and charge is stored in the capacitor. Capacitor will charge up to +2 V in our example.

During the negative cycle this voltage will be in series with the input voltage and gives total output -4V during negative peak of the input signal.

PROCEDURE:

1. Connect function generator with CRO. Set sine wave with 4V peak to peak. Ensure that offset voltage is 0.
2. Connect the function generator at the input of the clamping circuit
3. Observe output waveforms on the CRO for different clamping circuits and draw output waveforms.

PRECAUTIONS:-

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

RESULT:

Output waveform of clamper circuit is studied in CRO.

EXPERIMENT NO. 7

AIM:

To observe waveforms at the output of clipper circuit.

APPARATUS:

Diode
CRO
CRO PROBES
Resistor 1 kΩ
Breadboard
Connecting wires

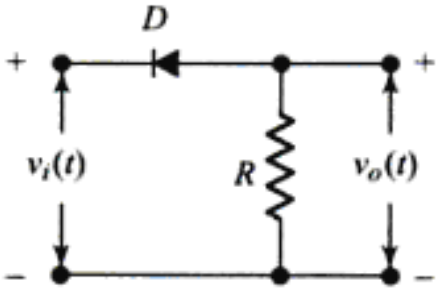
THEORY:

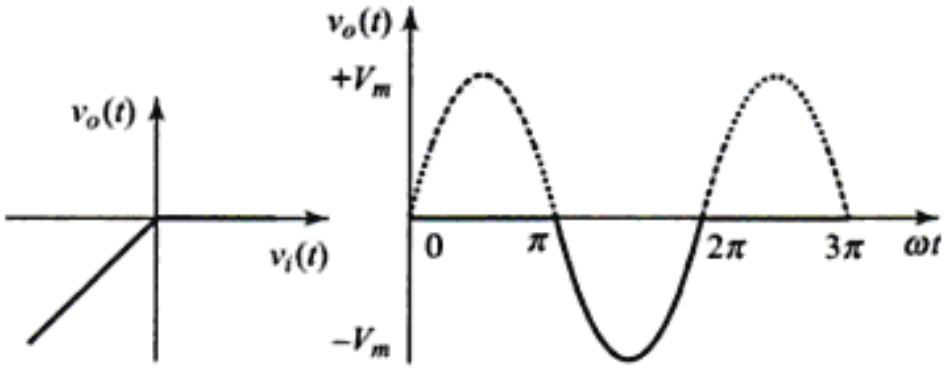
Clipping circuit is used to select for transmission that part of an arbitrary waveform which lies above or below some reference level. Clipping circuit "clips" some portion of the waveform. Clipping circuit is also referred to as voltage limiters.

Clamping circuit preserves shape of the waveform while clipping circuit does not preserve shape of waveform. Clipping circuit uses some reference level. Waveform above or below this reference level is clipped. Clipping circuits are also known as voltage limiter or amplitude limiter or slicers. Some clipper circuits are explained here.

Positive cycle clipper circuits:

Positive cycle clipper circuits are shown in the figure with series and shunt diode. Transfer characteristics and output waveform for sinusoidal input is shown.





For series diode:

- When $v_i(t)<0$, Diode D is in ON condition, input waveform is available at the output.
- When $v_i(t)>0$, Diode D is in OFF condition, input waveform is not available at the output and output remains zero.

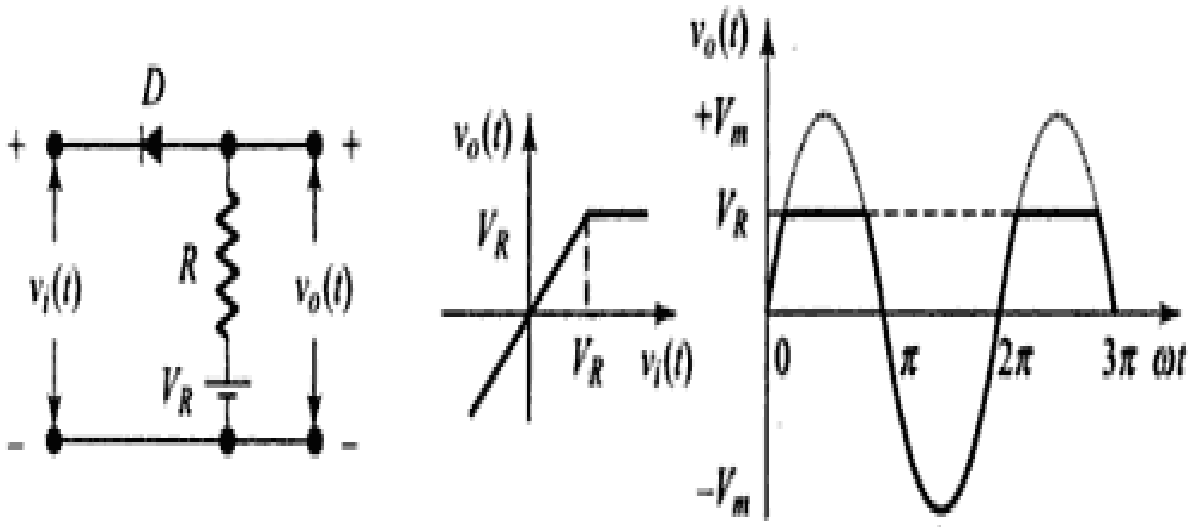
For shunt diode:

- When $v_i(t)<0$, Diode D is in ON condition which bypass the signal to the ground and hence input waveform is not available at the output.
- When $v_i(t)>0$, Diode D is in OFF condition and acts like an OFF switch, input waveform is available at the output.

For negative cycle clipper, polarity of diode is reverse.

Series diode positive clipping with positive reference:

In the circuit shown in the following figure, DC reference voltage is used. This is useful of we do not want to clip entire positive cycle but some portion of positive half cycle.

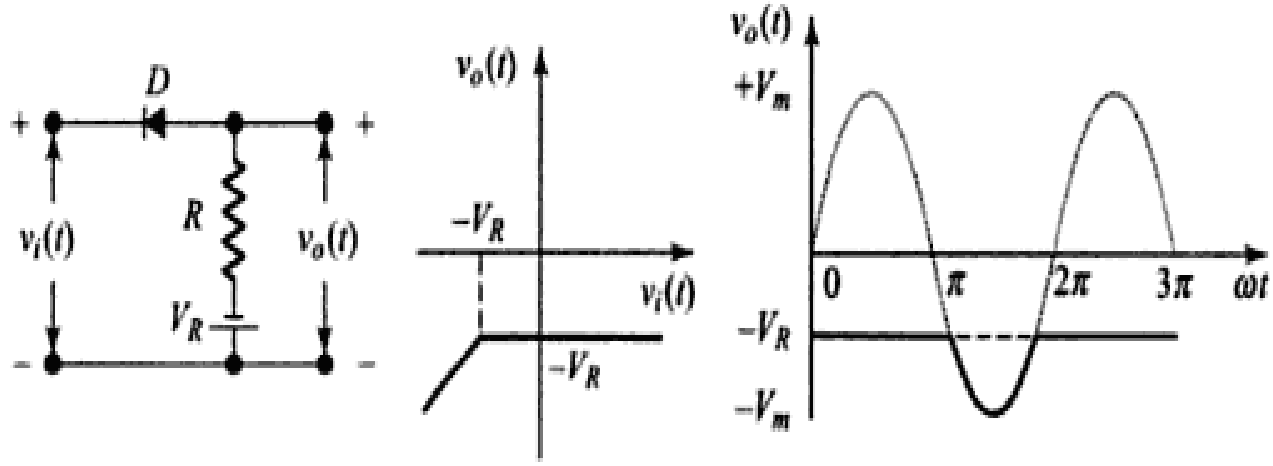


- When v_i (t)<V_R, Diode D is in ON condition, input waveform is available at the output.

- When v_i(t)> V_R, Diode D is in OFF condition, input waveform is not available at the output and output remains zero. Thus portion of output cycle clips as shown in the waveform.

Series diode positive clipping with negative reference:

If want to clip entire positive half cycle along with some portion of the negative cycle then negative DC reference can be used as shown in the following figure. In this case only some portion of negative cycle passes to the output.

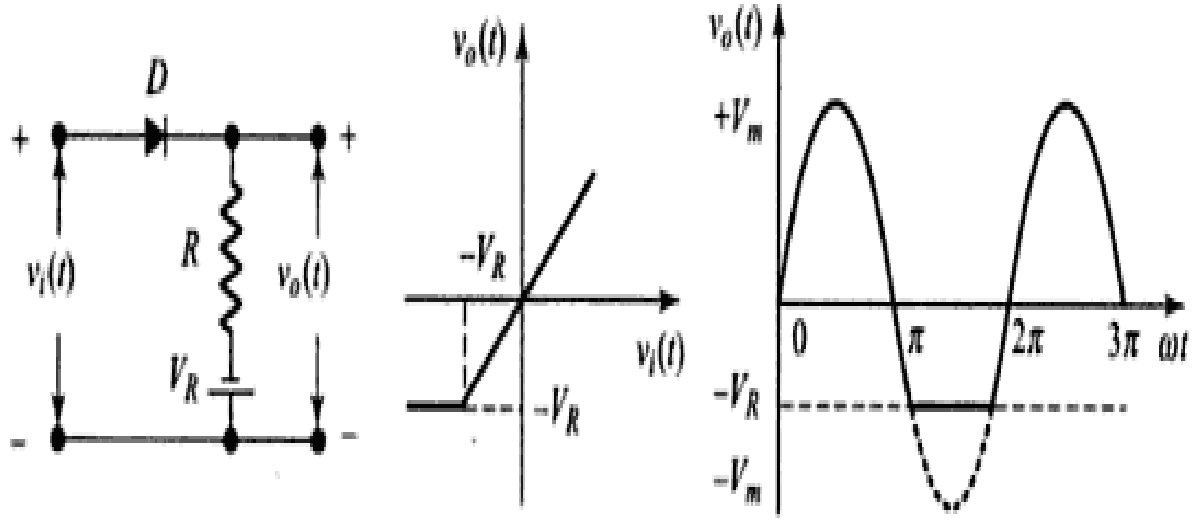


- When $v_i(t)<-V_R$, Diode D is in ON condition, input waveform is available at the output.

- When $v_i(t)> -V_R$, Diode D is in OFF condition, input waveform is not available at the output and output remains constant equal to V_R. Thus entire positive cycle and some portion of negative cycle below $-V_R$ clips.

Series diode negative clipping with reference:

Negative clipping can be achieved by changing polarity of the diode. Negative clipper with negative reference voltage is shown in the following figure. This will clip some portion of negative cycle.

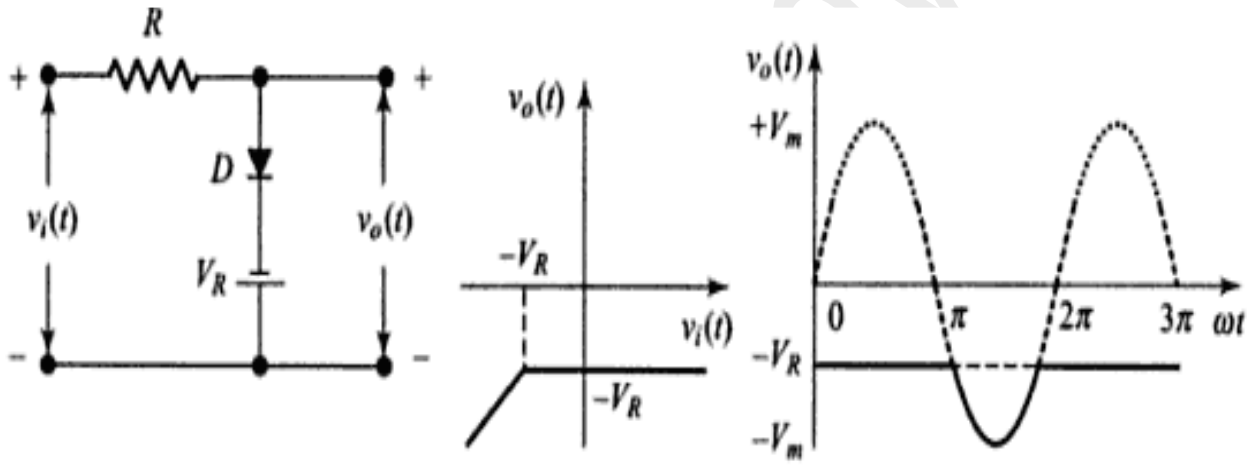


- When $v_i(t)>-V_R$, Diode D is in ON condition, input waveform is available at the output.

- When $v_i(t)< -V_R$, Diode D is in OFF condition, input waveform is not available at the output and output voltage remains constant which is equal to $-V_R$.

Shunt diode positive clipping with negative reference voltage:

Shunt diode positive clipping with negative reference voltage is as shown in the following circuit. This will clip entire positive cycle and some portion of negative cycle as shown in the waveform.

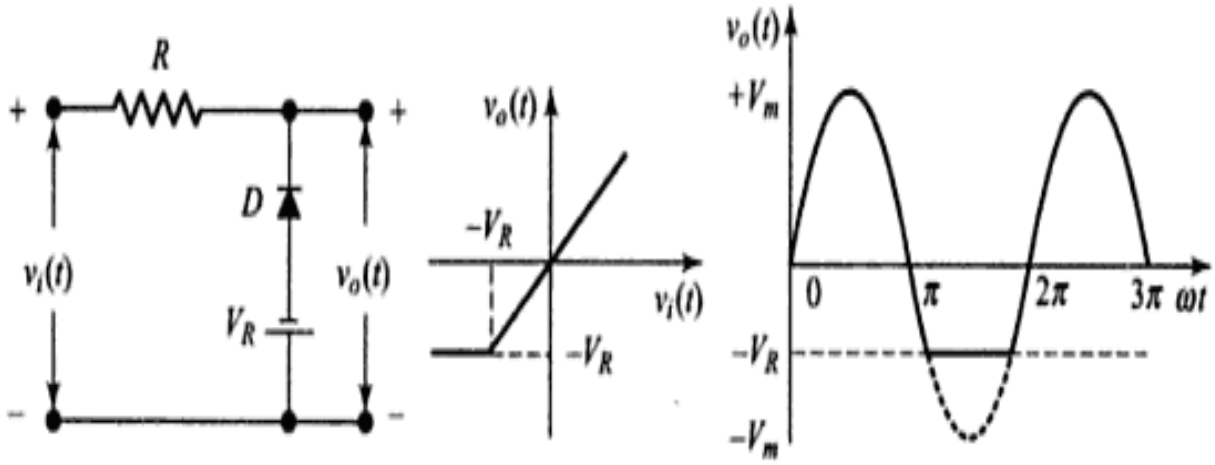


- When $v_i(t)<-V_R$, Diode D is in OFF condition (open circuit) and input waveform is available at the output.

- When $v_i(t)> -V_R$, Diode D is in ON condition, input waveform is not available at the output and negative voltage $-V_R$ is extended to the output. Output voltage remains constant equal to V_R. Thus entire positive cycle and some portion of negative cycle below $-V_R$ clips.

Shunt diode negative clipping with negative reference:

Negative clipping with negative reference voltage can be achieved by reversing polarity of the diode. Some portion of negative cycle clips.



- When $v_i(t) > -V_R$, Diode D is in OFF condition (open circuit) and input waveform is available at the output.

- When $v_i(t) < -V_R$, Diode D is in ON condition, input waveform is not available at the output and negative voltage $-V_R$ is extended to the output. Output voltage remains constant equal to V_R. Thus entire positive cycle and some portion of negative cycle below $-V_R$ clips.

PROCEDURE:

1. Connect function generator with CRO. Set sine wave with 6V peak to peak. Ensure that offset voltage is 0.
2. Connect the function generator at the input of the clipping circuit
3. Observe output waveforms on the CRO for different clipping circuits and draw output waveforms.

PRECAUTIONS:-

1. All the connections should be correct.
2. Parallax error should be avoided while taking the readings from the Analog meters.

RESULT:

Output waveform of different type of clipper circuit is studied in CRO.