LIST OF EXPERIMENTS

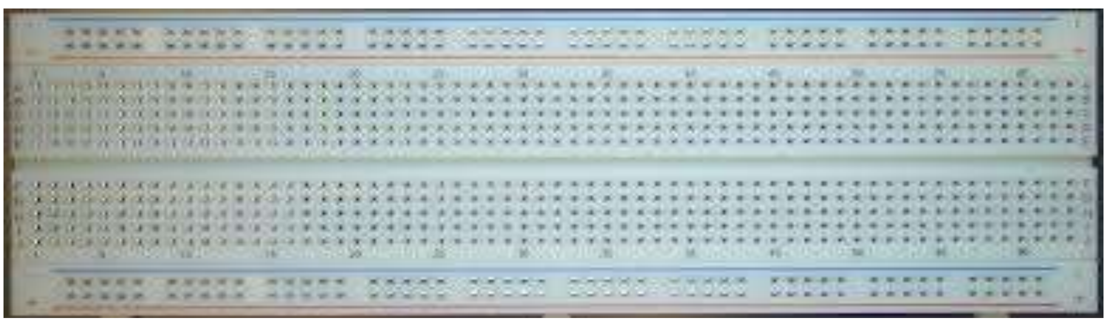
1. To Study basic electronics/ Electrical components.
2. Implement of the given Boolean function using logic gates in both SOP and POS
   Forms:
   a. Two input SOP - A.B + A’.B’
   b. Two input POS: - (A+B) (B+C) (A+C’)
3. To study about logic gates and verify their truth tables.
4. To design and construct half adder, full adder circuits and verify the truth table using logic gates
5. To design and construct half subtractor and full subtractor circuits and verify the truth table using logic gates.
6. To design, test and Verify BCD to Excess-3 code converter.
7. To design, test and verify BCD to 7 Segment display converter.
8. To design and verify the characteristic table of RS, and JK Flip flops.
9. To design and verify the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.
10. To realize and study of Shift Register.
    SISO (Serial in Serial out)
    SIPO (Serial in Parallel out)
    PIPO (Parallel in Parallel out)
    PISO (Parallel in Serial out)

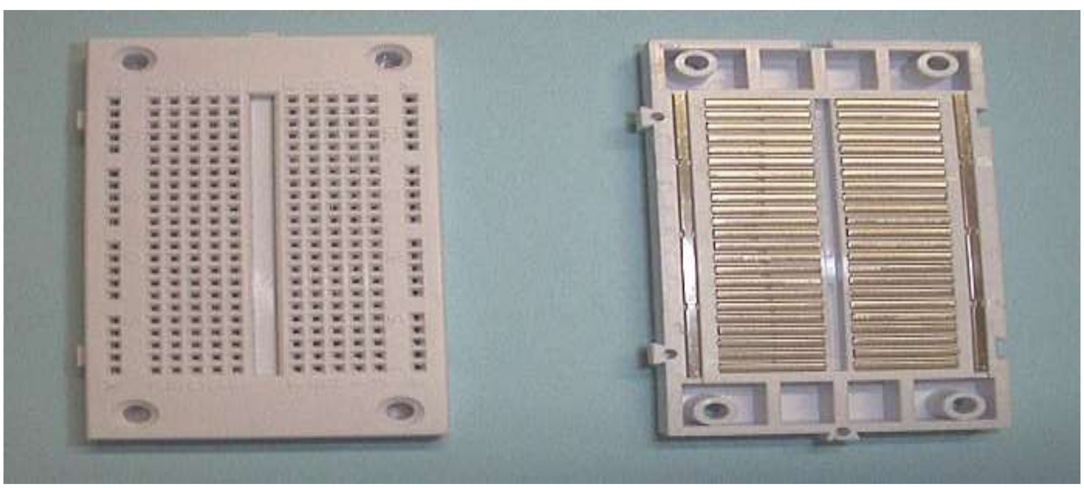
EXPERIMENT NO.-1

AIM: To Study basic electronics/ Electrical components.

THEORY: A breadboard (or protoboard) is usually a construction base for prototyping of electronics. The term "breadboard" is commonly used to refer to a solderless breadboard (plugboard).

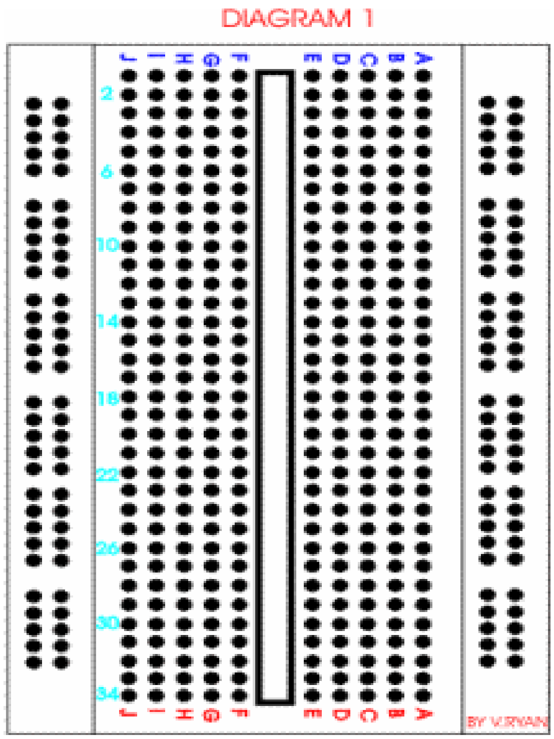
Because the solderless breadboard for electronics does not require soldering, it is reusable. This makes it easy to use for creating temporary prototypes and experimenting with circuit design. Older breadboard types did not have this property. A strip board (veroboard) and similar prototyping printed circuit boards, which are used to build semi-permanent soldered prototypes or one-offs, cannot easily be reused. A variety of electronic systems may be prototyped by using breadboards.





Breadboards are used to test circuits. Wires and components are simply pushed into the holes to form a completed circuit and power can be applied. One of the main advantages of using a breadboard is that the components are not soldered and if they are positioned incorrectly they can be moved easily to a new position on the board.

On the breadboard (diagram 1) seen opposite, letters are used to identify vertical columns and numbers to identify horizontal rows.



The red lines on diagram 2 show how some vertical columns and horizontal rows are internally connected. When power is applied to the breadboard current flows along these internal connections.

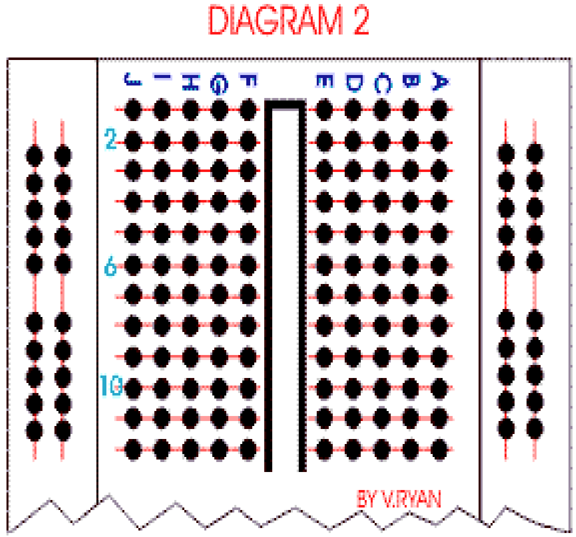
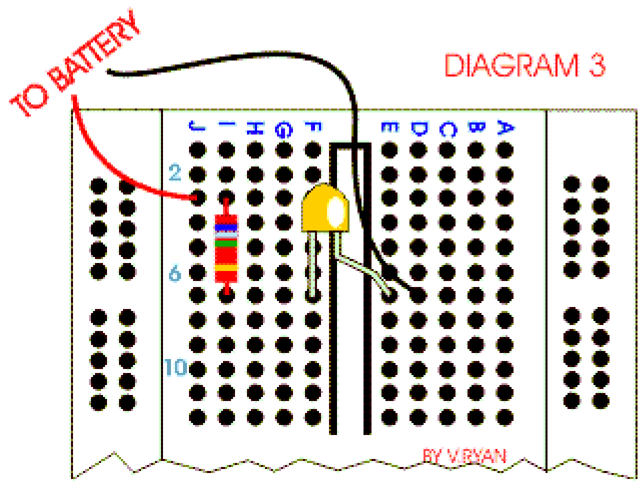
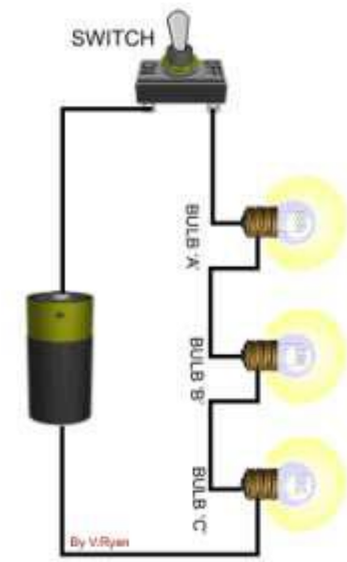
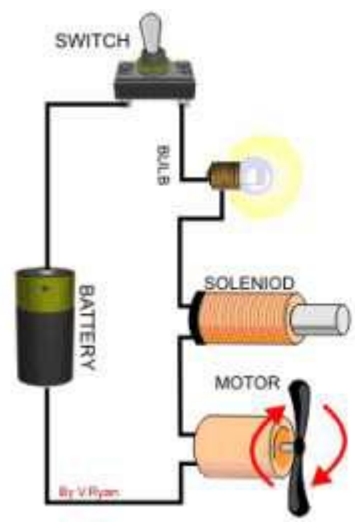


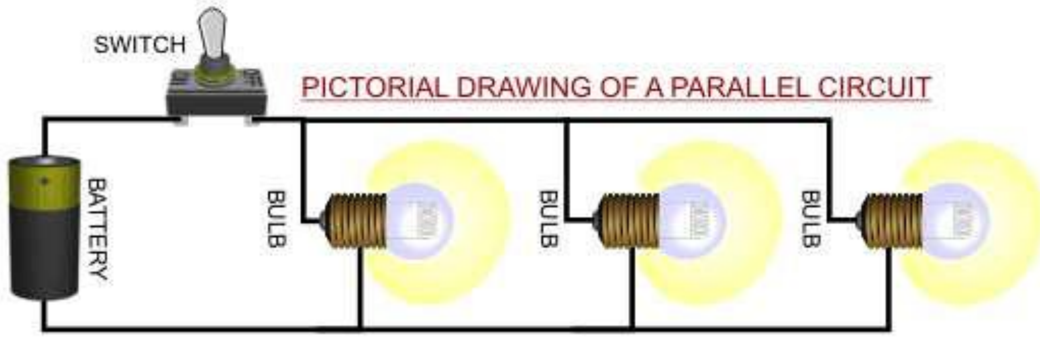
Diagram 3 shows how a 380 ohm resistor and an LED are setup on a breadboard. When a 9 volt battery is attached the LED lights. Try replacing the resistor with a higher value such as a 680 ohm resistor. The resistance will be greater and the LED should shine less bright.

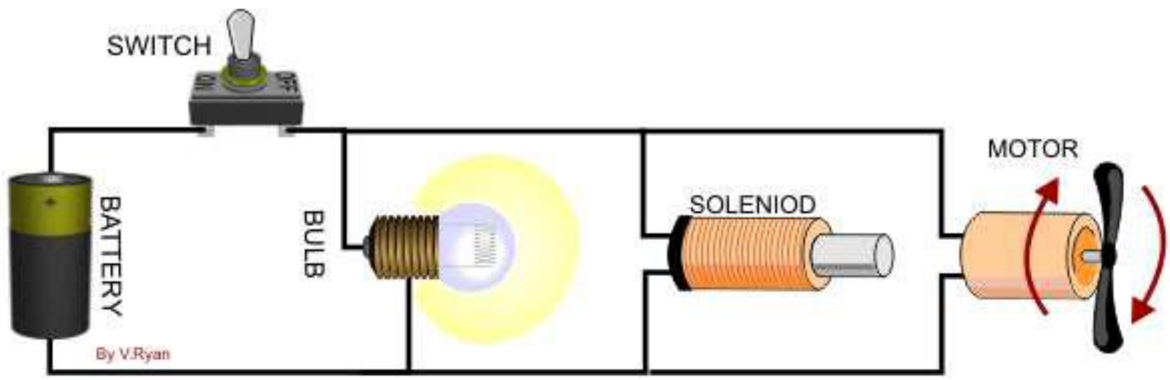


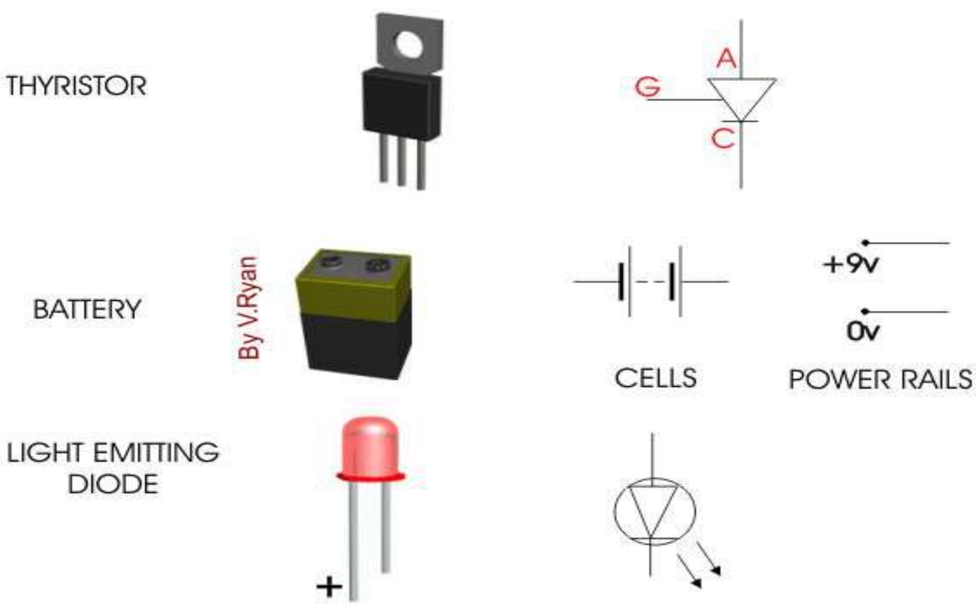




PICTORIAL DIAGRAM OF A SERIES CIRCUIT

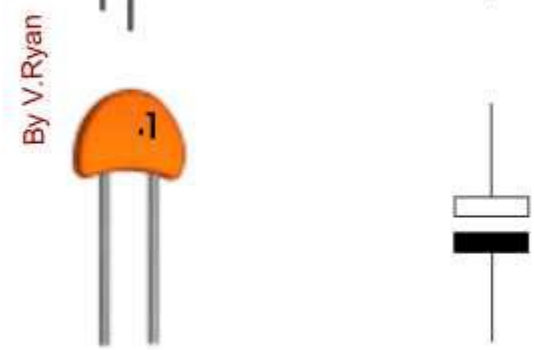

SWITCH
PICTORIAL DRAWING OF A PARALLEL CIRCUIT
BATTERY
BULB
BULB
BULB


SWITCH
MOTOR
SOLENIOD
BATTERY
BULB
By V.Ryan

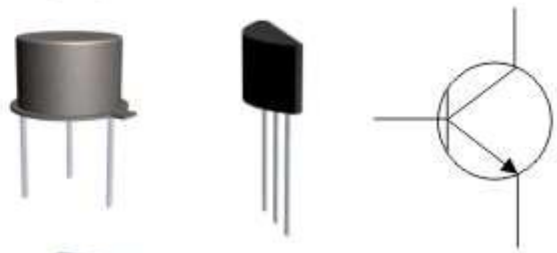

THYRISTOR
A
G
C
BATTERY
By V.Ryan
+9v
0v
CELLS
POWER RAILS
LIGHT EMITTING DIODE
+

ELECTROLYTIC
CAPACITOR

NON-ELECTROLYTIC
CAPACITOR

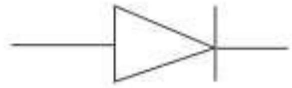


NPN TRANSISTOR

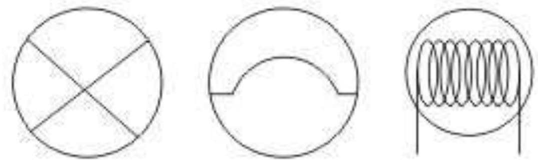


PNP TRANSISTOR

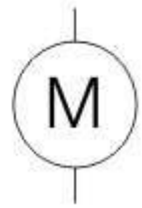
DIODE



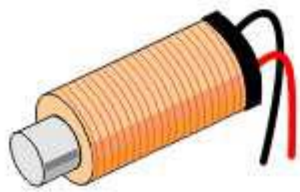
BULB / FILAMENT

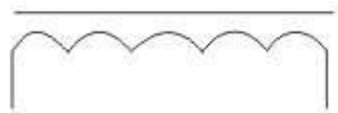


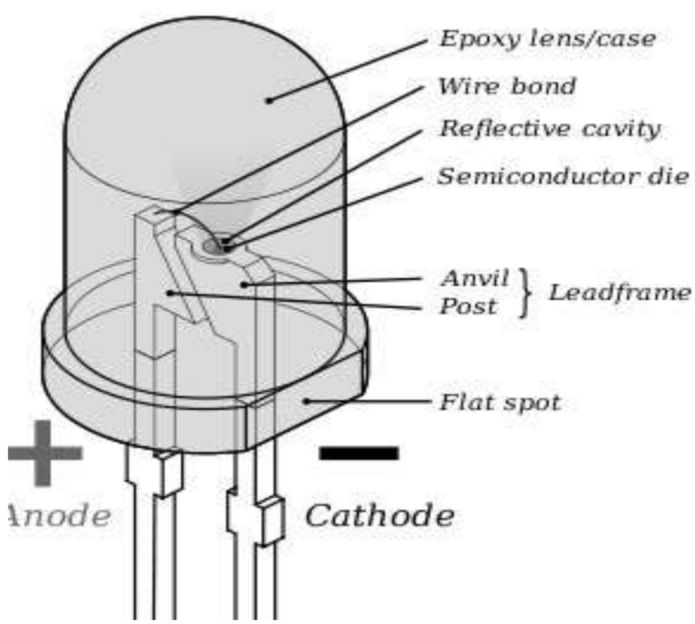
MOTOR



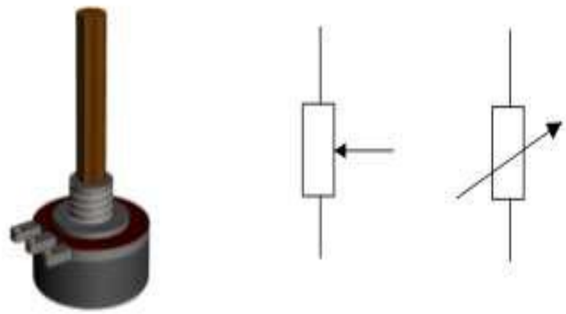
SOLENOID





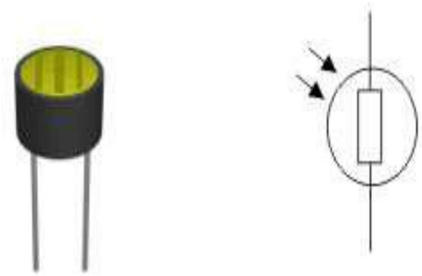


VARIABLE
RESISTOR



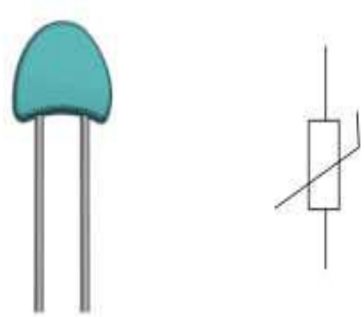
PRESET
RESISTOR

LDR /
LIGHT DEPENDENT
RESISTOR

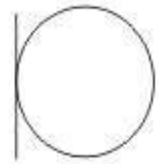


RESISTOR

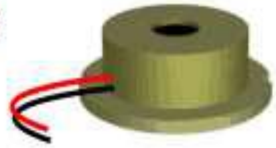
THERMISTOR



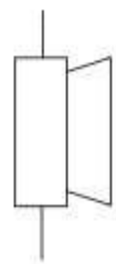
MICROPHONE



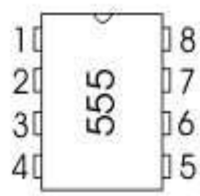
BUZZER



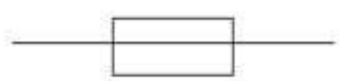
SPEAKER



IC
INTEGRATED CIRCUIT



FUSE



EXPERIMENT NO.-2

AIM

Implement of the given Boolean function using logic gates in both SOP and POS Forms:

Two input SOP - A.B + A’.B’

Two input POS: - (A+B) (B+C) (A+C’)

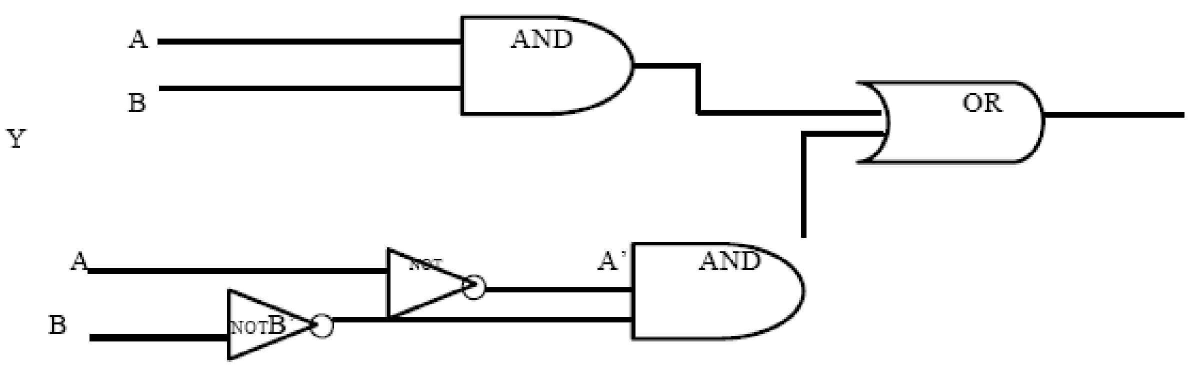
APPARATUS REQUIRED: Digital Lab Kit, Single Strand Wires, ICs, breadboards, Connecting Wires.

THEORY:

a) **SOP**: - It is the Sum of product form in which the terms are taken as 1. It is denoted in the K-map expression by sigma (∑)

<u>A.B. + A’B’</u>

LOGIC CIRCUIT OF THE EXPRESSION:



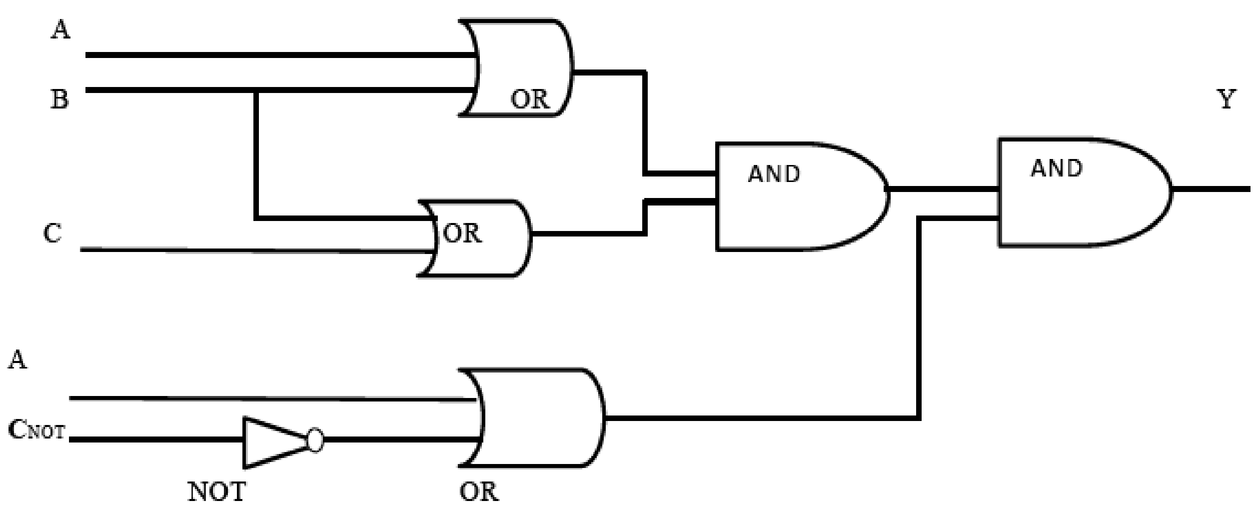
TRUTH TABLE SOP EXPRESSION:

A	B	A'	B'	A.B	A'.B'	Y= AB' + AB'
0	0	1	1	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

b) **POS**: - It is the product of the sums form in which the terms are taken as 0. It is denoted in the K-Map expression by the Sign pie (π)

(A+B) (B+ C) (A + C')

LOGIC CIRCUIT OF THE EXPRESSION:



TRUTH TABLE POS EXPRESSION:

A	B	C	A+B	B+C	A+C'	Y= (A+B)(B+C)(A+C')
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	1	1	1	1
0	1	1	1	1	0	0
1	0	0	1	0	1	0
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

For SOP form: - A.B + A'.B'

1. Place the Digital lab kit at one place.
2. Take the one AND gate ICs i.e. IC no.7408, one NOT gate IC i.e. IC no. 7404 and one OR gate IC i.e. IC no. 7432.
3. Place these 3 ICs in the breadboard one by one.
4. Now, connect the AND gate with the inputs of A and B and other AND gate in the same IC is given by the complement input of the A and B i.e. A' and B' by using NOT gate with the help of connecting wires.
5. Give the output voltage Vcc and GROUND to all the ICs separately.
6. When whole configuration is read, gently on the switch and note there output of different values of A and B i.e. either 0 or 1.

For POS form :- (A+B)(B+C)(A+C')

1. Place the Digital lab kit at one place.
2. Take the 1 **OR**, 1 **AND**, 1 **NOT** gates IC
3. Place these 3 ICs in the breadboard one by one.
4. Now, connect the OR gate of Input A or B, B or C and last one is A or C'

(i.e. complement of C using NOT gate. Inputs are connected with the help of connecting wires.

5. When whole circuit is complete, on the switch and note down the output with different values of A, B and C.

Result:- Hence, given Boolean Expression is implemented by the Logic Gates. i.e.

(i) A.B + A'.B'

(ii) (A+B) (B+C) (A+C')

EXPERIMENT NO. -3

AIM:

To study about logic gates and verify their truth tables.

APPARATUS REQUIRED: Breadboard, Logic Gate IC's, Power supply, connecting wires

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE:

`The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR GATE:

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

PROCEDURE:

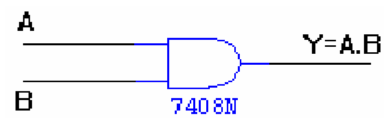
(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

AND GATE:

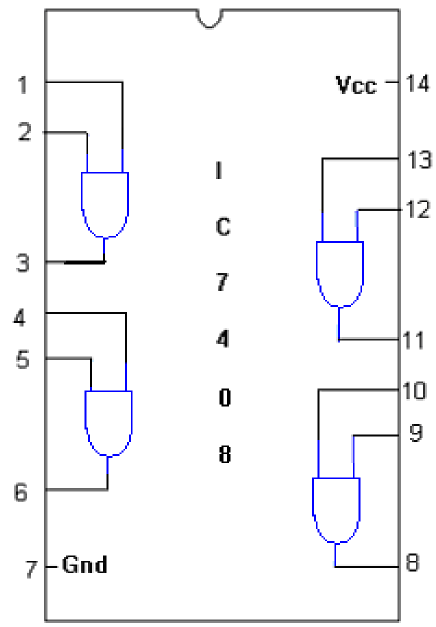
SYMBOL:



TRUTH TABLE

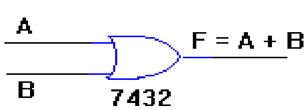
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

PIN DIAGRAM:



OR GATE:

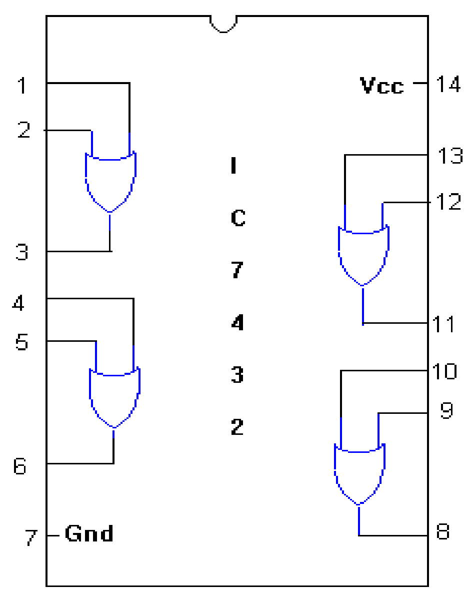
SYMBOL :



TRUTH TABLE

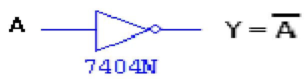
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

PIN DIAGRAM :



NOT GATE:

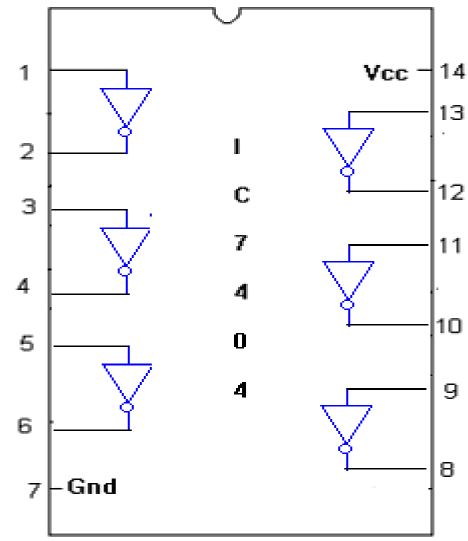
SYMBOL:



TRUTH TABLE :

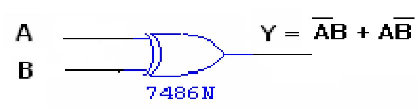
A	$\overline{A}$
0	1
1	0

PIN DIAGRAM:



X-OR GATE :

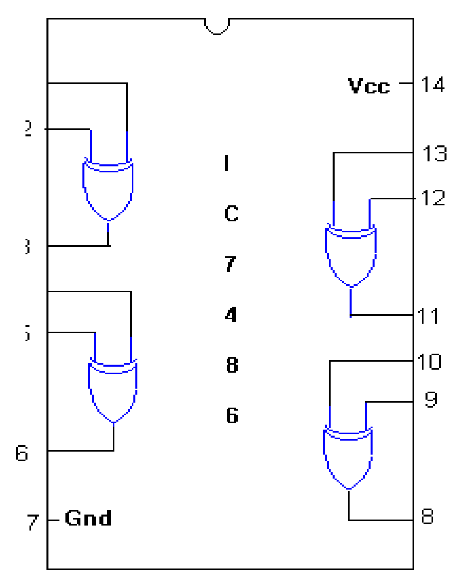
SYMBOL :



TRUTH TABLE :

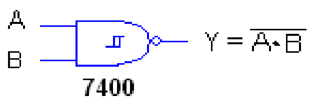
A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM :



2-INPUT NAND GATE:

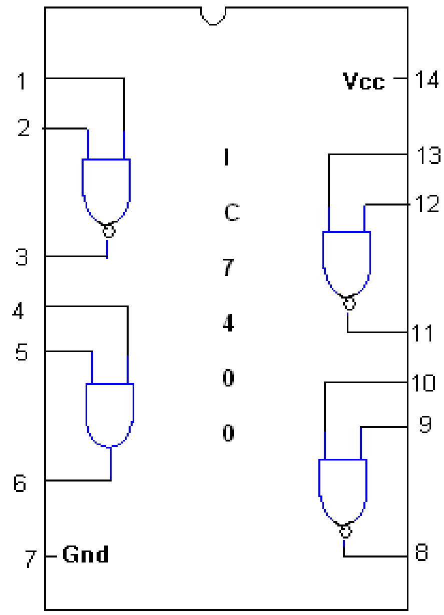
SYMBOL:



TRUTH TABLE

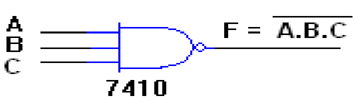
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM:



3-INPUT NAND GATE :

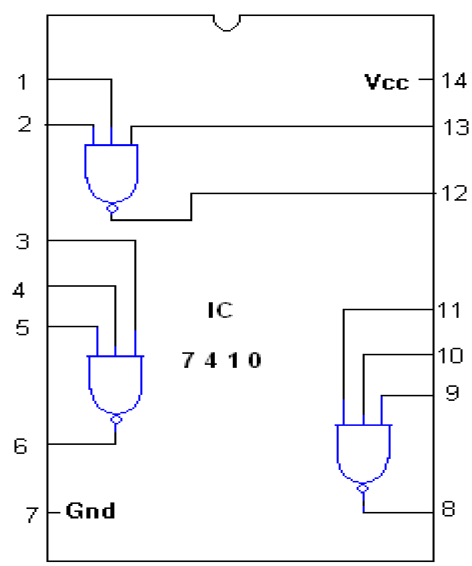
SYMBOL :



TRUTH TABLE

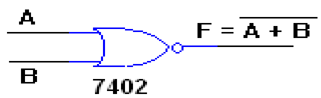
A	B	C	$\overline{A.B.C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

PIN DIAGRAM :



NOR GATE:

SYMBOL :



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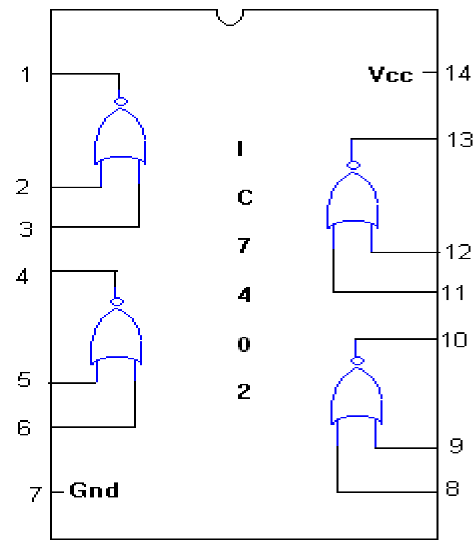


TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

RESULT: The logic gates are verified.

EXPERIMENT NO. -4

AIM:

To design and construct half adder, full adder circuits and verify the truth table using logic gates.

APPARATUS REQUIRED: Breadboard, Logic Gate IC’s, Power supply, connecting wires

THEORY:

HALF ADDER:

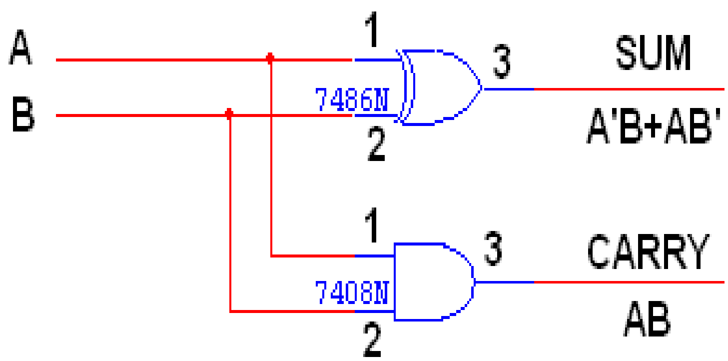
A half adder has two inputs for the two bits to be added and two outputs one from the sum ‘ S’ and other from the carry ‘ c’ into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

LOGIC DIAGRAM:

HALF ADDER

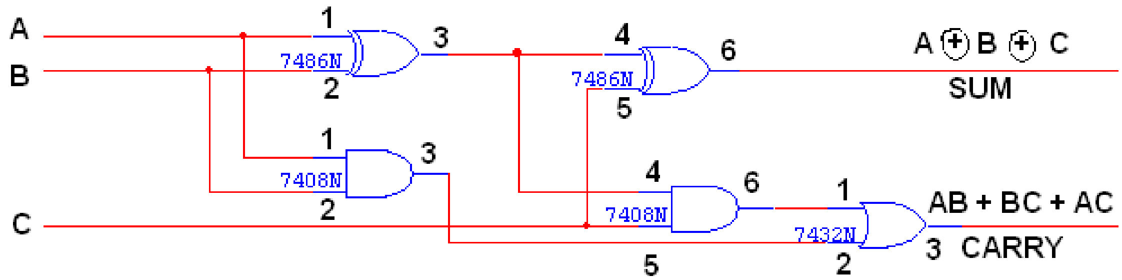


TRUTH TABLE:

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

<u>**FULL ADDER**</u>

FULL ADDER USING TWO HALF ADDER



TRUTH TABLE:

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT: Adders are verified.

EXPERIMENT NO. -5

AIM:

To design and construct half subtractor and full subtractor circuits and verify the truth table using logic gates.

APPARATUS REQUIRED: Breadboard, Logic Gate IC's, Power supply, connecting wires

HALF SUBTRACTOR:

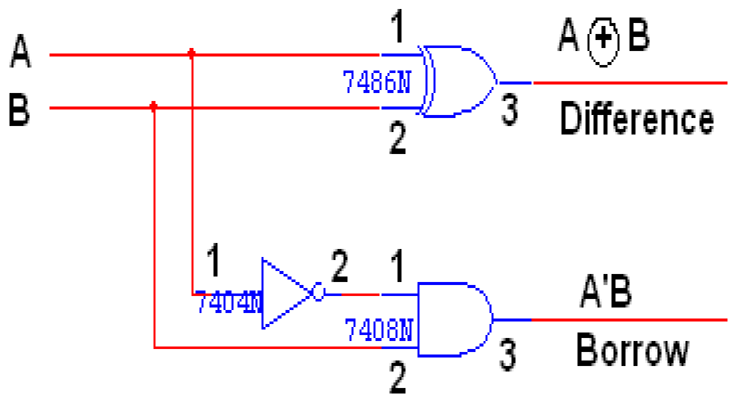
The half subtractor is constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR Gate, borrow output can be implemented using an AND Gate and an inverter.

FULL SUBTRACTOR:

The full subtractor is a combination of X-OR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor .The first half subtractor will be C and A B. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term is the inverted difference output of first X-OR.

LOGIC DIAGRAM:

HALF SUBTRACTOR



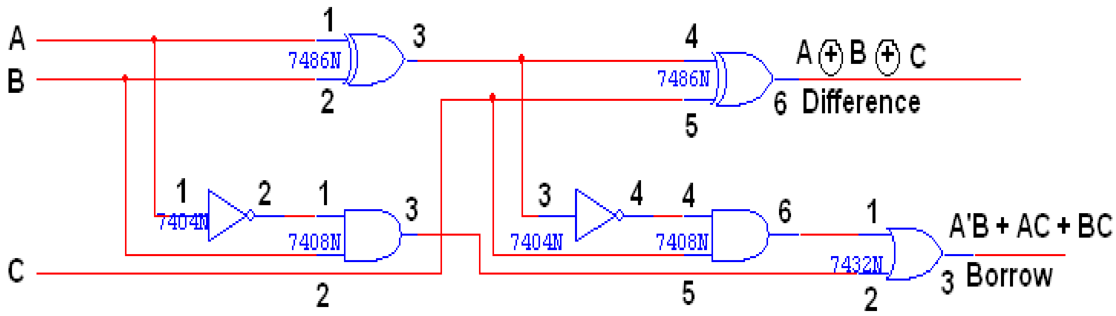
TRUTH TABLE:

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

LOGIC DIAGRAM:

FULL SUBTRACTOR

FULL SUBTRACTOR USING TWO HALF SUBTRACTOR:



TRUTH TABLE:

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

PROCEEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT: Subtractor is verified.

EXPERIMENT NO-6

AIM:
To design, test and Verify BCD to Excess-3 code converter.

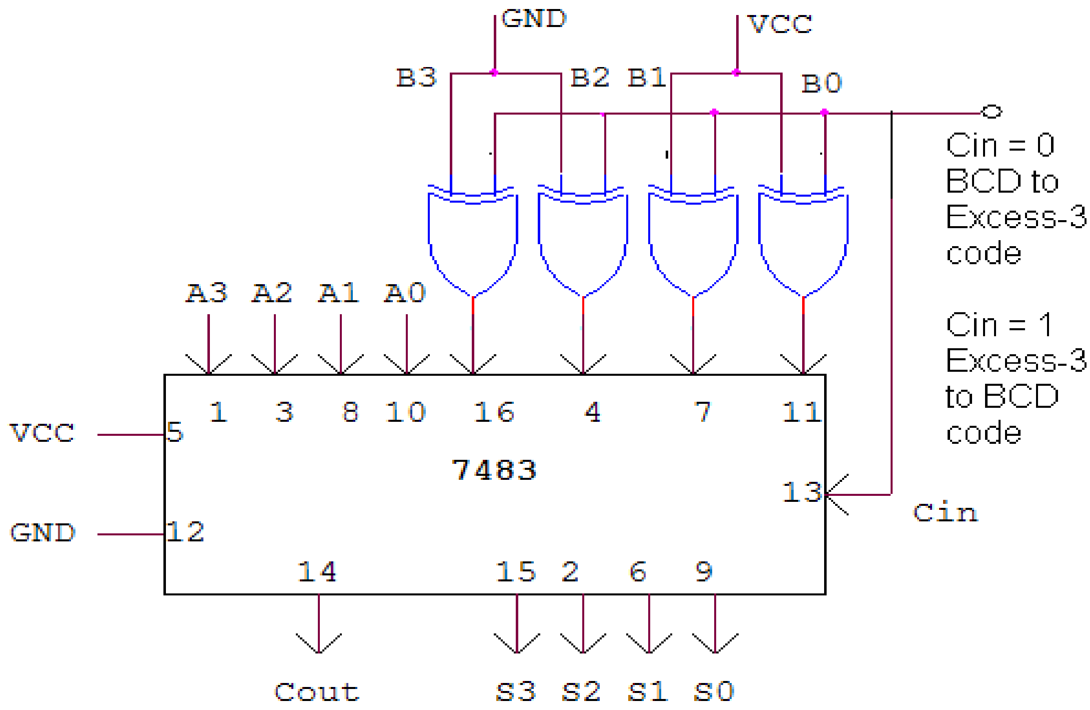
APPARATUS REQUIRED:
IC 7483, IC 7486, Patch cords & IC trainer kit

THEORY:
Code converter is a combinational circuit that translates the input code word into a new corresponding word. The excess-3 code digit is obtained by adding three to the corresponding BCD digit. To Construct a BCD-to-excess-3-code converter with a 4-bit adder feed BCD code to the 4-bit adder as the first operand and then feed constant 3 as the second operand. The output is the corresponding excess-3 code. To make it work as a excess-3 to BCD converter, we feed excess-3 code as the first operand and then feed 2's complement of 3 as the second operand. The output is the BCD code.

BCD TO EXCESS-3 CONVERTOR
TRUTH TABLE:

BCD input				Excess – 3 output			
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

LOGIC DIAGRAM:



PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Apply BCD code as first operand(A) and binary 3 as second operand(B) and cin=0

Realizing BCD-to-Excess-3-code:

- Apply Excess-3-code code as first operand(A) and binary 3 as second operand(B) and Cin=1 for realizing Excess-3-code to BCD.
- Verify the Truth Table and observe the outputs.

RESULT: Realized BCD code to Excess-3 code conversion using 7483 IC

EXPERIMENT NO-7

AIM:

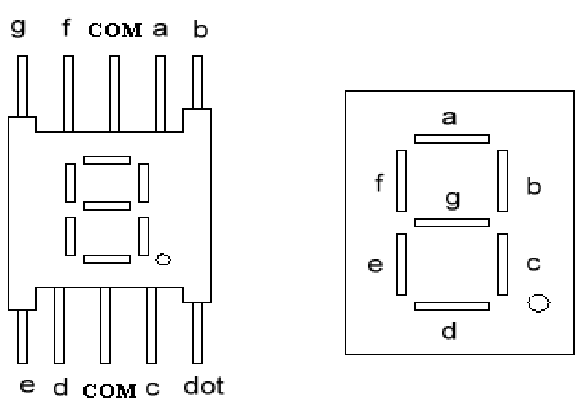
To design, test and verify BCD to 7 Segment display converter.

Apparatus Required:

IC7447, 7-Segment display (common anode), Patch chords, resistor (1K) & IC Trainer Kit

THEORY:

The Light Emitting Diode (LED) finds its place in many applications in these modern electronic fields. One of them is the Seven Segment Display. Seven-segment displays contains the arrangement of the LEDs in "Eight" (8) passion, and a Dot (.) with a common electrode, lead (Anode or Cathode). The purpose of arranging it in that passion is that we can make any number out of that by switching ON and OFF the particular LED's. Here is the block diagram of the Seven Segment LED arrangement. The Light Emitting Diode (LED), finds its place in many applications in this modern electronic fields. One of them is the Seven Segment Display. Seven-segment displays contains the arrangement of the LEDs in "Eight" (8) passion, and a Dot (.) with a common electrode, lead (Anode or Cathode). The purpose of arranging it in that passion is that we can make any number out of that by switching ON and OFF the particular LED's. Here is the block diagram of the Seven Segment LED arrangement.

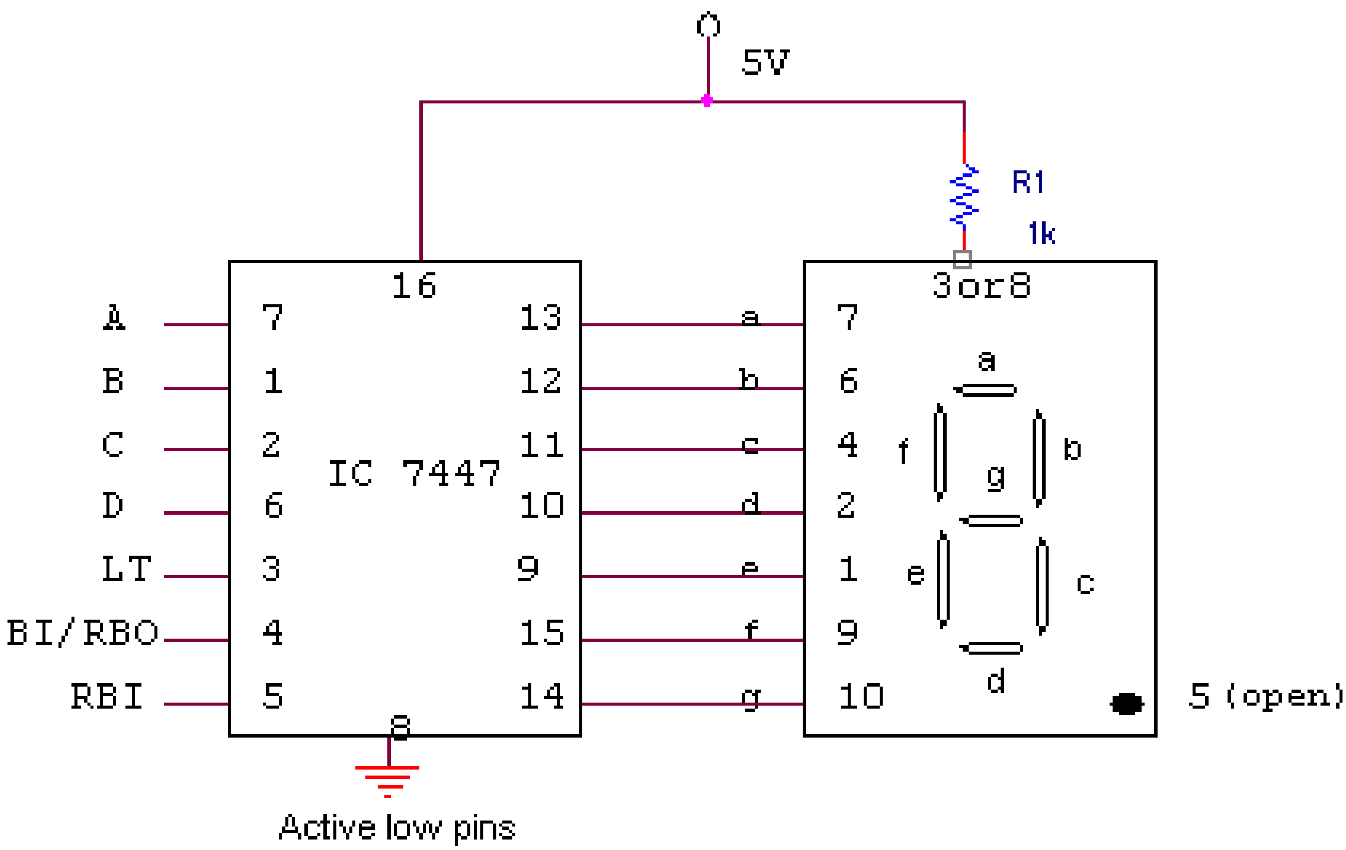


Seven-Segment Display

LED's are basically of two types-

Common Cathode (CC) -All the 8 anode legs uses only one cathode, which is common. Common Anode (CA)-The common leg for all the cathode is of Anode type. A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2n unique output lines. The IC7447 is a BCD to 7-segment pattern converter. The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code.

CIRCUIT DIAGRAM:



TRUTH TABLE:

BCD Inputs				Output Logic Levels from IC 7447 to 7-segments							Decimal number display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

RESULT:

Realized BCD to 7 Segment display converter.

EXPERIMENT NO-8

AIM:

To design and verify the characteristic table of RS, and JK Flip flops.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	NOR gate	IC 7402	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7411	
5.	NAND gate	IC 7400	
6.	Connecting wires		As required

THEORY:

A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

RS FLIP FLOP:

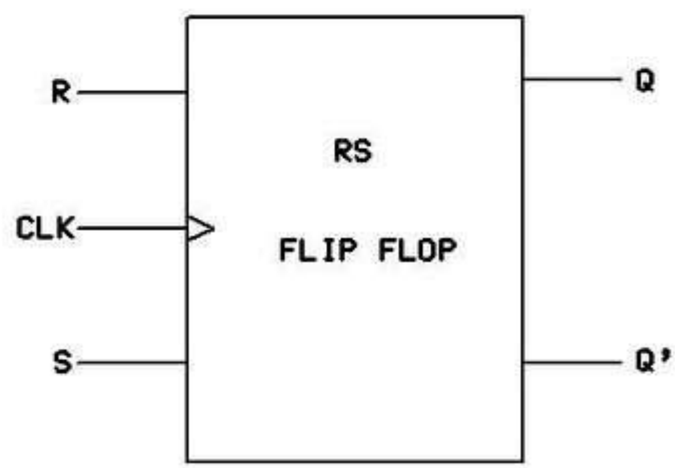
The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form. The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

JK FLIP FLOP:

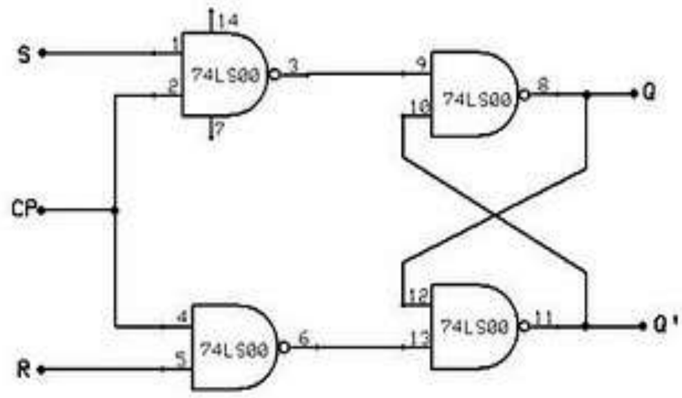
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q' is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

RS FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

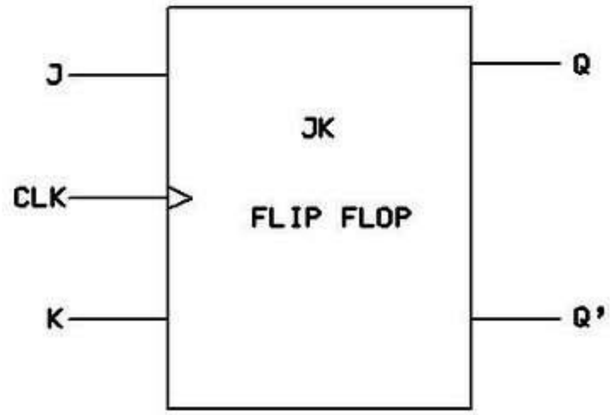


CHARACTERISTIC TABLE:

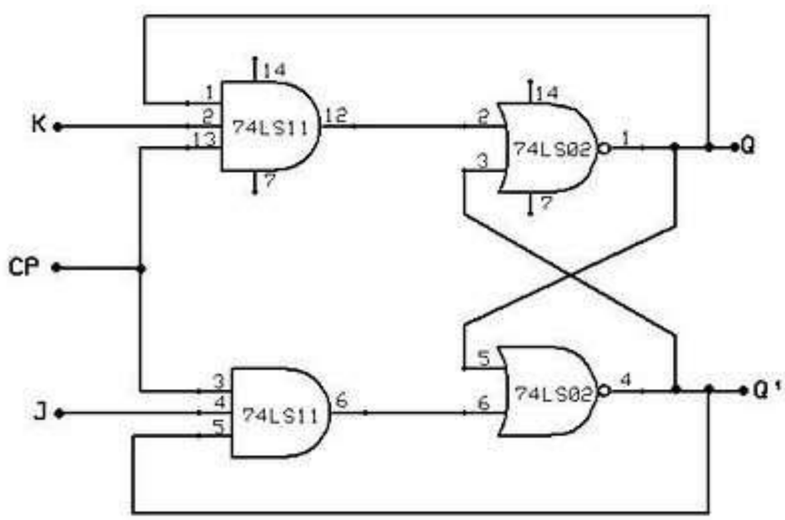
CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	S	R			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	X	
8	1	1	1	X	

JK FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	J	K			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	0	

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and observe the status of all the flip flops.

RESULT:

The Characteristic tables of RS and JK flip flops were verified.

EXPERIMENT NO. -9

AIM: To design and verify the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	OR gate	IC 7432	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7411	
5.	Connecting wires		As required

THEORY:

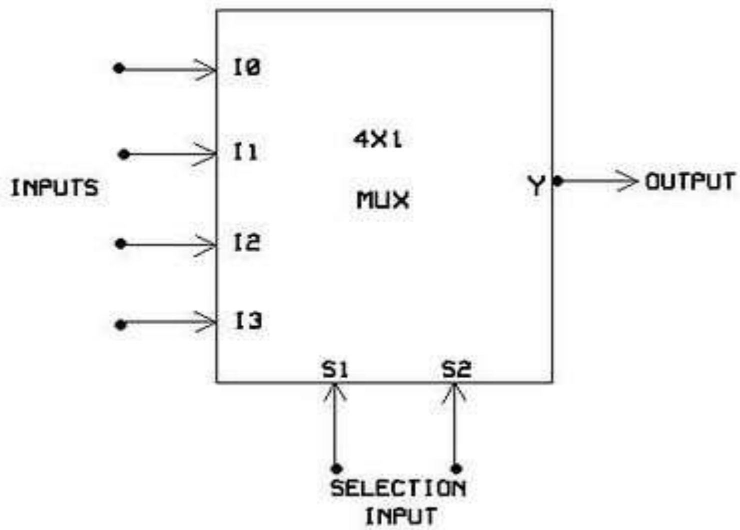
Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

DESIGN:

4 X 1 MULTIPLEXER

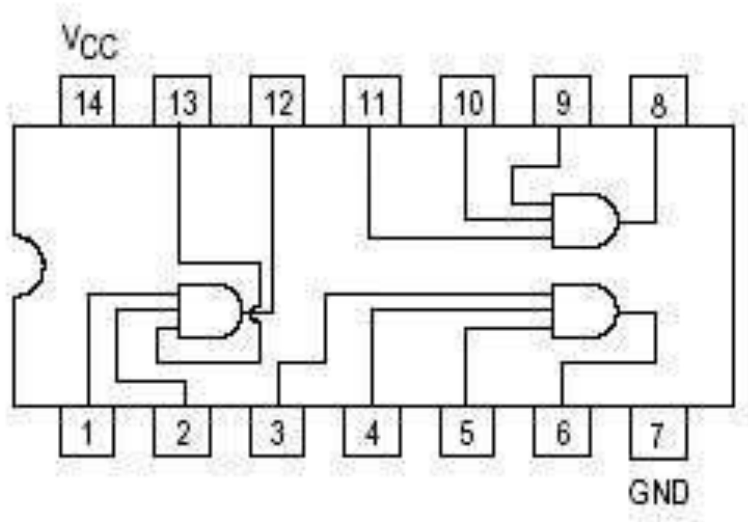
LOGIC SYMBOL:



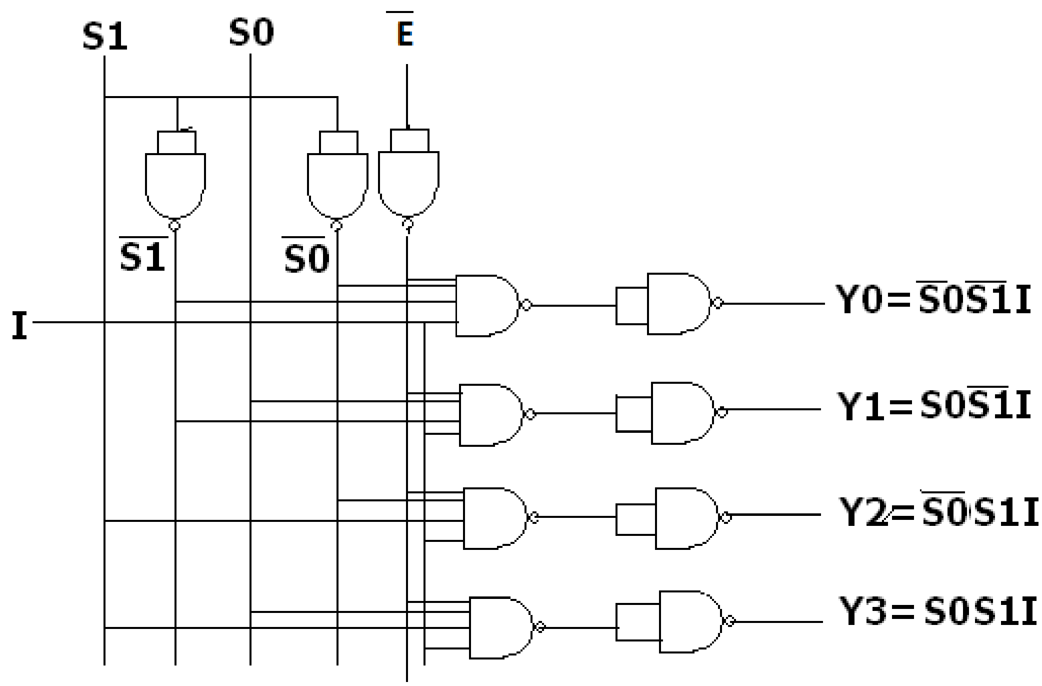
TRUTH TABLE:

S.No	SELECTION INPUT		OUTPUT
	S1	S2	Y
1.	0	0	I_0
2.	0	1	I_1
3.	1	0	I_2
4.	1	1	I_3

PIN DIAGRAM OF IC 7411:

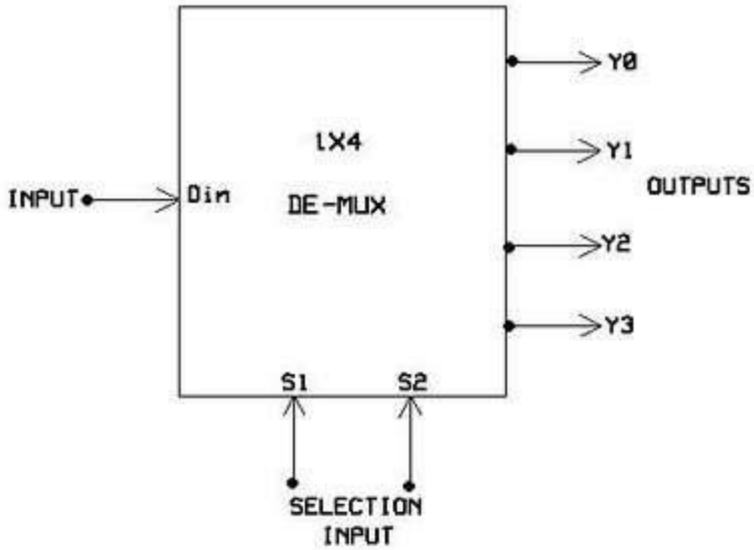


CIRCUIT DIAGRAM:



1X4 DEMULTIPLEXER

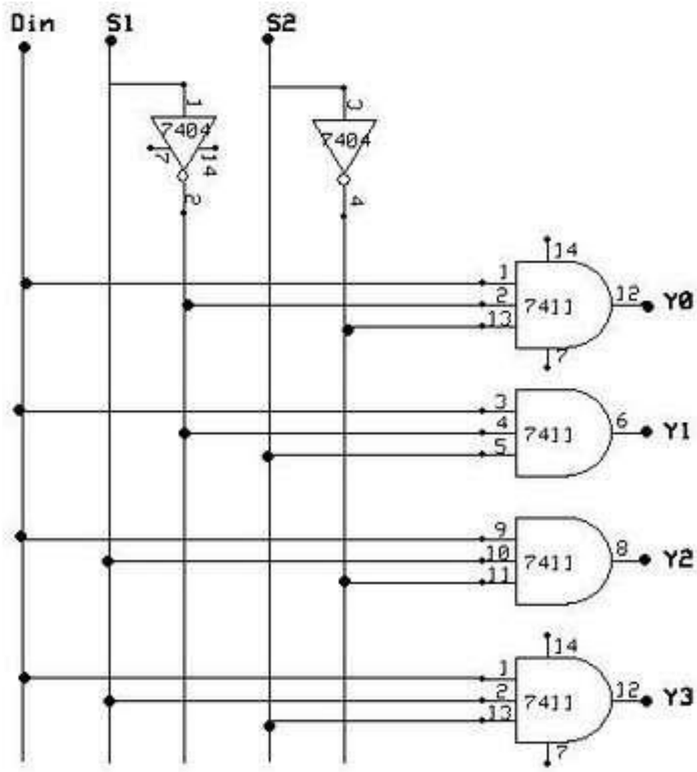
LOGIC SYMBOL:



TRUTH TABLE:

S.No	INPUT			OUTPUT			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the multiplexer & Demultiplexer.

RESULT:

The design of the 4x1 Multiplexer and 1x4 Demultiplexer circuits was done and their truth tables were verified.

EXPERIMENT NO-10

AIM:

To realize and study of Shift Register.

1) SISO (Serial in Serial out)
2) SIPO (Serial in Parallel out)
3) PIPO (Parallel in Parallel out)
4) PISO (Parallel in Serial out)

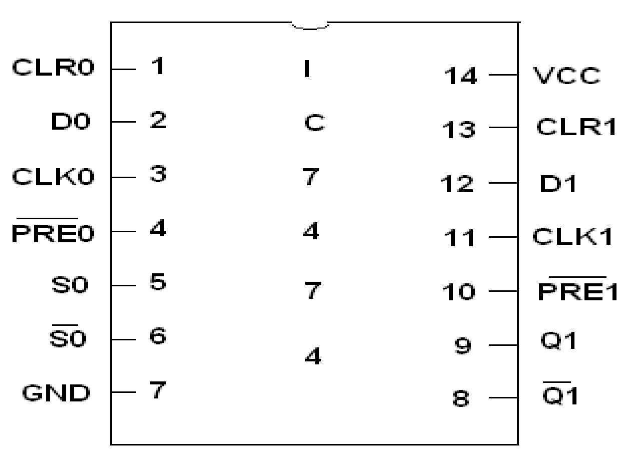
Apparatus Required:

D flip flop IC 7474 -2, or gate IC 7432 -1, IC trainer kit – 1, patch cords - 35

THEORY:

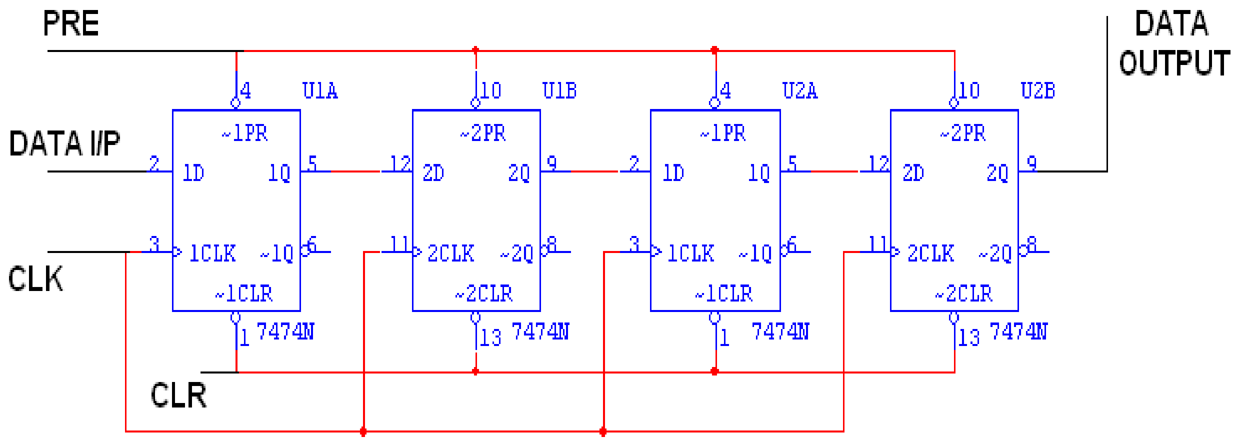
A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

PIN DIAGRAM



LOGIC DIAGRAM:

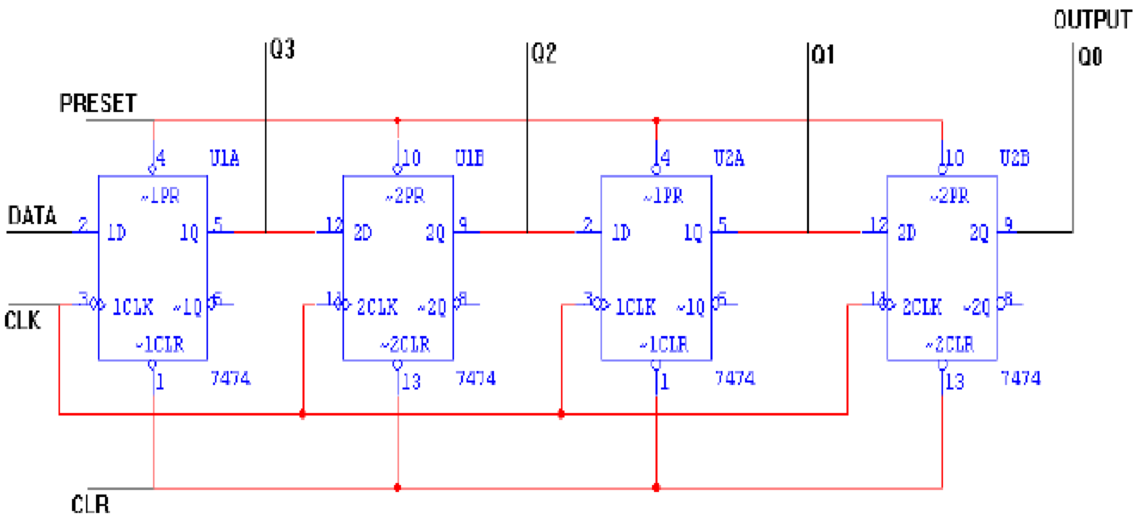
SERIAL IN SERIAL OUT:



TRUTH TABLE:

CLK	Serial in	Serial out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

LOGIC DIAGRAM:
SERIAL IN PARALLEL OUT:

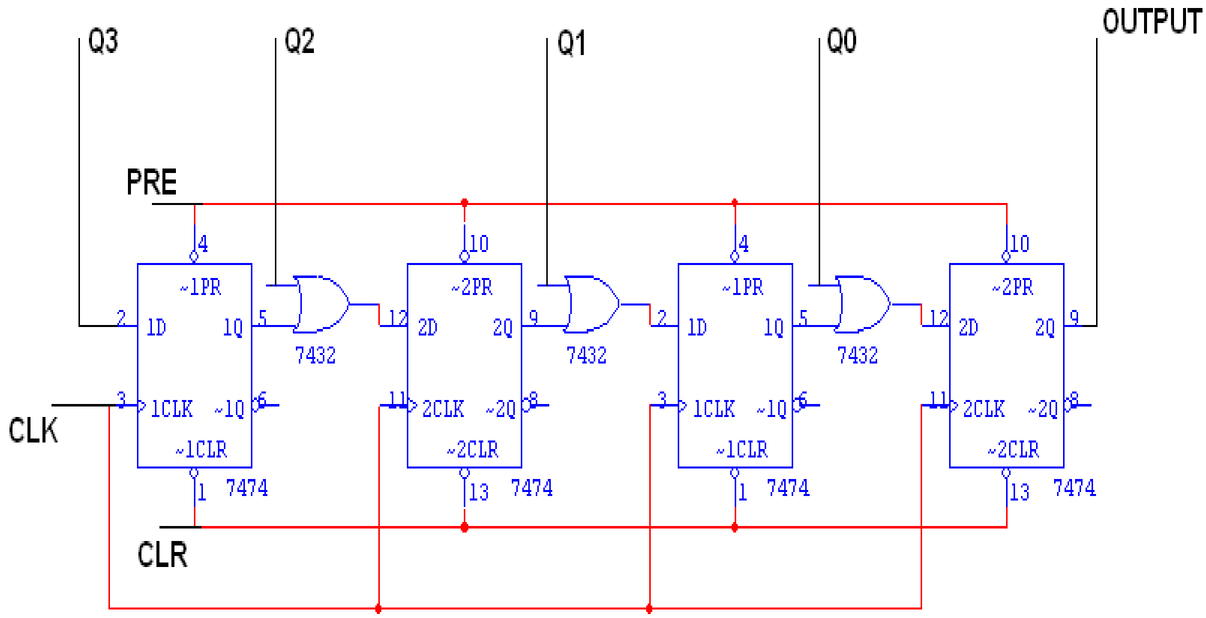


TRUTH TABLE:

CLK	DATA	OUTPUT			
		Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	1
4	1	1	0	0	1

LOGIC DIAGRAM:

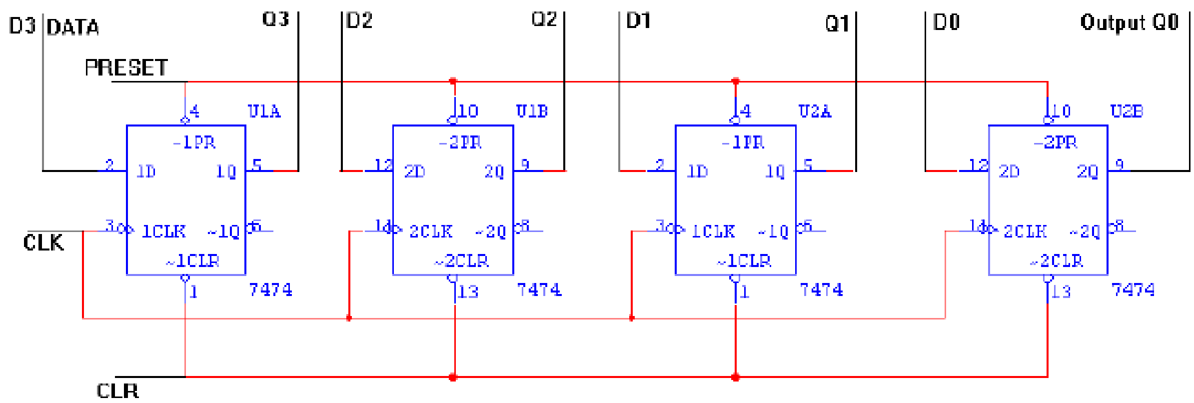
PARALLEL IN SERIAL OUT:



TRUTH TABLE:

CLK	Q3	Q2	Q1	Q0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

LOGIC DIAGRAM:
PARALLEL IN PARALLEL OUT:



TRUTH TABLE:

CLK	DATA INPUT				OUTPUT			
	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

PROCEDURE:
(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

RESULT: Realized various Shift register.